1/28/03 EIC2800

B5420 5256

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

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Date 1/28/03 Serial # 09/998,387 Priority Application Date 12/5/00

Your Name M. Lewis Examiner # 73172

AU 2829 Phone 305-3743 ~~Room~~ Plaza 3-380D

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-9

Problem:

See Page 2 lines 6-33

" " 3 " 1

Solution:

" " " " 4-33

" " " " 1

Also utilize the same compounds as illustrated in pages 8-10 for the insulating base, wiring layer, etc. →

Staff Use Only	Type of Search	Vendors
Searcher: Derrick Blalock	Structure (#)	STN ✓
Searcher Phone:	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 1/30/03	Fulltext	Lexis-Nexis
Date Completed: 1/31/03	Patent Family	WWW/Internet
Searcher Prep/Rev Time:	Other	Other
Online Time:		

01/30/2003

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     FILE 'WPIX, JAPIO, INPADOC' ENTERED AT 11:10:37 ON 30 JAN 2003
L1            0 S JP2601128/PN

     FILE 'HCAPLUS' ENTERED AT 11:13:44 ON 30 JAN 2003
                E CIRCUIT SUBSTRATE/CT
                E CIRCUIT SUBSTRATES/CT

     FILE 'INSPEC' ENTERED AT 11:14:12 ON 30 JAN 2003
                E CIRCUIT SUBSTRATES/CT
L2            0 S CIRCUIT SUBSTRATES/CT
L3          243 S CIRCUIT SUBSTRATE

     FILE 'HCAPLUS' ENTERED AT 11:15:30 ON 30 JAN 2003
                E RESIN/CT
                E RESINS/CT
                E E3+ALL/CT
L4         3561 S CIRCUIT SUBSTRATE
L5          869 S THERMOSET? EPOXY RESIN
L6            1 S L4 AND L5
L7       142106 S EPOXY RESIN
L8          318 S L4 AND L7
L9         2887 S CIRCUIT(W)(LAYER? OR FILM OR COAT?)
L10           2 S L9 AND L5
```

L14 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:340963 HCAPLUS
DN 127:43664
TI Multilayer printed circuit board having interstitial via hole and its manufacture
IN Urasaki, Naoyuki; Ogawa, Nobuyuki; Shimizu, Masahiro; Tsuru, Yoshiyuki; Nakaso, Akishi
PA Hitachi Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09092981	A2	19970404	JP 1995-249259	19950927
PRAI	JP 1995-249259		19950927		

AB The board has interstitial via hole (IVH) penetrating .gtoreq.2 of multiple **circuit layers** which are elec. insulated by heat-resistant resin intermediate layers. Manuf. of the structure by repeating a process comprising following successive steps is also claimed; (1) bonding a plate corresponding to an inner layer and an outer Cu foil by using an inserted thermosetting film including a bifunctional epoxy resin and halogenated bifunctional phenols assocd. with a hardener and a polyfunctional epoxy resin, (2) selective etching to form fine holes on the Cu foil, (3) removing the resist, (4) removing the cured resin below the fine holes by an etchant comprising an amide solvent, an alkali metal compd., and an alc. to form via holes, (5) plating for connecting the inner plate and the Cu foil, (6) forming a circuit on the Cu foil by selective etching through a resist, and (7) removing the resist.

L14 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:624847 HCAPLUS
DN 117:224847
TI Chargeable particle containing electric conductor similar to electrophotographic developer toner for printed circuit
IN Isozaki, Seiya; Sugimoto, Mitsuhiro; Ooshima, Tsutomu
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04237064	A2	19920825	JP 1991-4902	19910121
PRAI	JP 1991-4902		19910121		

AB The title particle has (1) a globular core at least comprising elec. conductive metal particle dispersion in the 1st resin, which is not softened under temp. and pressure in following hot press process after fixing on a **circuit substrate**, and (2) a shell of the 2nd resin, which is softened at a temp. lower than the temp. of fixing. The particle, e.g., a composite of **thermosetting epoxy resin** core and a heat-fusible acrylic resin shell, is used similarly to electrophotog. developer toner to prep. printed circuit.

L14 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:237476 HCAPLUS
DN 116:237476
TI One-liquid **thermosetting epoxy resin** compositions containing polymercaptans for coatings with improved pot life
IN Yano, Katsumi; Futakuchi, Tomoaki; Mizumoto, Fujitoshi
PA Toyama Prefecture, Japan; Asahi Chemical Research Laboratory Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04001219	A2	19920106	JP 1990-101764	19900419
PRAI	JP 1990-101764		19900419		

AB Title compns. for low temp.- and rapidly curable moisture-resistant coatings, useful for elec. or electronic parts, contain prepolymers from .gtoreq.2 epoxy group-contg. compds. and heterocyclic imidazoles and reaction products of polymercaptans, metal chelating compds., and succinic acid (I). Thus, Epikote 807 100, EMI 24 CN 20, and dimethylbenzene 20 parts were treated in the presence of a Pt catalyst at 90.degree. for 12 h, treated with a mixt. of Q 11 (polymercaptan) 8, Al(III) acetylacetonate (II) 2, and I 0.008 part at 50.degree. for 24 h to give the title compn. showing pot life 6 mo vs. 10 days for the compn. without I and II.

FILE 'WPIX, JAPIO'

L1 40429 S CIRCUIT(1N)(SUBSTRATE OR LAYER? OR FILM OR COAT?)

L2 53834 S (WIRING OR WIRE)(1N)(LAYER? OR FILM OR COAT?)

L3 128755 S (EPOXY RESIN OR BISPHENOL OR DIPHENYLOLMETHANE OR EPICHLOROHYDRIN OR EPOXIDE RESINSOR EPOXY COMPOUNDS OR EPOXY POLYMERS OR EPOXY RESINS)

L4 2365 S UNCURED(2N) RESIN

L5 40 S METAL?(2N) COHESION

L6 16 S (TOMEKAWA S OR TOMEKAWA, S OR TOMEKAWA SATORU OR TOMEKAWA, SATORU)/AU

L7 529 S (YAMASHITA, Y OR YAMASHITA Y OR YAMASHITA, YOSHIHISA OR YAMASHITA YOSHIHISA)/AU

L8 2 S (CN1364049 OR JP2002237677 OR EP1213952 OR US2002066961)/PN

L9 13 S DE2155029/PN OR DE2413158/PN OR EP734065/PN OR DE2536152/PN OR DK143289/PN OR EP12094/PN OR EP645950/PN OR EP734576/PN OR EP74605/PN S EP768334/PN OR EP786808/PN OR EP851726/PN OR EP855720/PN OR ES2136556/PN OR ES2149699/PN OR FR2443787/PN OR JP10107445/PN

L10 8 S DE2155029/PN OR DE2413158/PN OR EP734065/PN OR DE2536152/PN OR DK143289/PN OR EP12094/PN OR EP645950/PN OR EP734576/PN OR EP74605/PN S EP768334/PN OR EP786808/PN

L11 4 S DE2155029/PN OR DE2413158/PN OR EP734065/PN OR DE2536152/PN OR DK143289/PN

L12 4 S EP12094/PN OR EP645950/PN OR EP734576/PN OR EP74605/PN S EP768334/PN OR EP786808/PN

L13 6 S EP12094/PN OR EP645950/PN OR EP734576/PN OR EP74605/PN OR EP768334/PN OR EP786808/PN

L14 6 S EP851726/PN OR EP855720/PN OR ES2136556/PN OR ES2149699/PN OR FR2443787/PN OR JP10107445/PN

L15 9 S NL175324/PN OR US6143116/PN OR AT321668/PN OR AT7404112/PN OR AU7245021/PN OR AU7247998/PN OR AU7583954/PN OR AU9852728/PN

L16 8 S AU9884144/PN OR CA2187857/PN OR CH606485/PN OR CN1075338/PN OR CN1108026/PN OR CN1137324/PN OR CN1195001/PN OR CN1302179/PN

L17 7 S CN1364049/PN OR DE3543924/PN OR EP1001852/PN OR EP1087261/PN OR EP1096842/PN OR EP1194025/PN OR EP1213952/PN OR FR2147337/PN

L18 5 S FR2158256/PN OR FR2159848/PN OR GB1395887/P

N OR GB1412986/PN OR GB1468065/PN OR GB1525012/PN OR GB1531327/
PN OR HU156112/PN

L19 20 S HU156458/PN OR IT961766/PN OR JP02258337/PN OR JP02281686/PN OR JP03116894/PN OR JP04001219/PN OR JP04094187/PN OR JP04169002/PN OR JP04237064/PN OR JP04372194/PN OR JP05009309/PN OR JP05082929/PN

L20 13 S JP05206598/PN OR JP06013754/PN OR JP0602165 5/PN OR "JP06034435 B4"/PN OR JP06052715/PN OR "JP06080894 B4"/PN OR JP06122785/PN OR JP06220368/PN

L21 14 S JP06283830/PN OR "JP07034506 B4"/PN OR JP07147464/PN OR JP07173448/PN OR JP07211145/PN OR JP07226110/PN OR JP08236884/PN OR JP08259912/PN

L22 10 S JP08307058/PN OR JP08330181/PN OR JP0833035 6/PN OR JP09046011/PN OR JP09092981/PN

L23 6 S JP09232471/PN OR JP09232705/PN OR JP0924671 6/PN

L24 6318 S (SUZUKI, TAKESHI OR SUZUKI TAKESHI OR SUZUKI, T OR SUZUKI T)/AU

L25 55 S (KAWAKITA, YOSHIHIRO OR KAWAKITA YOSHIHIRO OR KAWAKITA Y OR KAWAKITA, Y)/AU

L26 3383 S (NAKAMURA T OR NAKAMURA, T OR NAKAMURA TADASHI OR NAKAMURA, TADASHI)/AU

L27 92 S (L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23)

L28 40393 S L1 NOT L27

L29 242 S L28 AND INSULAT?(W) BASE

L30 40 S L29 AND L2

L31 3 S L30 AND (ELECTRICAL?(W)(CONNET? OR JOIN? OR CONDUCTIV?))

L32 75408 S (ELECTRICAL?(W)(CONNET? OR JOIN? OR CONDUCTIV?))

L33 0 S L30 AND BOND?(W) STRENGTH

L34 1 S L30 AND ((L3 OR L4 OR L5))

L35 14 S L30 AND CONDUCTOR

L36 1622 S L28 AND L2

L37 36 S L36 AND L3

L38 415 S L36 AND CONDUCTOR

L39 0 S L37 AND L32

L40 2 S L38 AND L4

L41 0 S L38 AND L5

L42 10 S L38 AND GLASS TRANSITION

L43 0 S L30 AND GLASS TRANSITION

L44 1 S L38 AND BONDING(W) SITE

L45 16 S L28 AND L4

L46	43	S	L31 OR L34 OR L35 OR L40 OR L44 OR L45 OR L42
L47	23	S	L30 NOT (L31 OR L34 OR L35 OR L40 OR L44 OR L45 OR L42)
L48	10245	S	(L6 OR L7 OR L24 OR L25 OR L26) NOT ((L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23) OR L27)
L49	52	S	L48 AND L1
L50	10	S	L49 AND ((L2 OR L3 OR L4 OR L5))
L51	1	S	L49 AND L32
L52	11	S	L50 OR L51

L46 ANSWER 5 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2001-127265 [14] WPIX
DNN N2001-093950 DNC C2001-037299
TI Ceramic circuit board for hybrid integrated circuit, has copper coating electrode layer with peak portion formed at predetermined height from **insulated base** surface at the edge of front **wiring conductor layer.**
DC L03 U14 V04
PA (KYOC) KYOCERA CORP; (NPDE) NIPPONDENSO CO LTD
CYC 1
PI JP 2000286522 A 20001013 (200114)* 6p
ADT JP 2000286522 A JP 1999-92101 19990331
PRAI JP 1999-92101 19990331
AB JP2000286522 A UPAB: 20010312
NOVELTY - Front **wiring conductor layer** (2) comprising tungsten or molybdenum, is formed on an **insulated base** (1). Copper coating electrode layer (8) and thick film resistor (5) are formed on front **wiring conductor layer**, sequentially. Height from **insulated base** surface in edge of the layer (2) to peak of copper coating layer, is set to 2-15 mu m. Thickness of copper coating layer at peak position is set to 2-12 mu m.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for ceramic circuit board manufacturing method.
USE - For hybrid integrated circuit and semiconductor package.
ADVANTAGE - Reduces the variation in the resistance value of the thick film resistor formed over the copper coating layer. Enables to perform resistance adjustment by laser trimming simply and correctly. Improves manufacturing yield of the substrate and obtains a reliable ceramic wiring board.
DESCRIPTION OF DRAWING(S) - The figure shows the expanded sectional view of the principal part of the ceramic circuit board.
Insulated base 1
Wiring conductor layer 2
Thick film resistor 5
Electrode layer 8
Dwg.1/2

L46 ANSWER 6 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2000-667032 [65] WPIX
DNN N2000-494405 DNC C2000-202239
TI Multilayered printed wiring board comprising polyaryl ketone resin and amorphous polyether and formed by fusing of layers and making through holes and wiring.
DC A26 A85 L03 V04
PA (MISD) MITSUBISHI PLASTICS IND LTD; (NPDE) NIPPONDENSO CO LTD
CYC 1
PI JP 2000200976 A 20000718 (200065)* 10p
ADT JP 2000200976 A JP 1999-577 19990105
PRAI JP 1999-577 19990105
AB JP2000200976 A UPAB: 20001214
NOVELTY - A multilayered printed wiring board has a film-like insulating material consisting of a polyaryl ketone resin having a crystalline fusion peak temperature of 260 degrees C or higher, 65-35 percent by weight, and an amorphous polyether imide resin, 35-65 percent by weight.
DETAILED DESCRIPTION - Double sided-through holes are formed in the film-like insulating material. A conductive paste is filled in the through holes to form a thermal fusing film for interlayer connection for a laminated electrical circuit. A **conductor** foil is thermally fused to the single surface or both the surfaces of the thermal fusing

film to form **circuits**. A **film**-like **wiring** substrate is provided. A laminated material consisting of the **film**-like **wiring** substrate and the thermal fusing film is prepared. The laminated materials are alternately superimposed and are integrated by thermal fusion.

USE - The method produces the multilayered printed wiring board.

ADVANTAGE - The thermoplastic resin composition for constituting each layer exerts superior adhesive strength in thermal fusion. The multilayered printed wiring board having four or more layers has no delamination. Heat resistance inherent in the thermoplastic resin composition exerts required soldering heat resistance.

Dwg.0/2

L46 ANSWER 7 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2000-614249 [59] WPIX
CR 2000-415509 [34]; 2001-524778 [26]
DNN N2000-454980 DNC C2000-183954
TI Multi **layer wiring** board for portable telephone, video camera, has multi-interconnection layer structure whose thermal expansion coefficient difference with that of core wiring board is equal to preset value.
DC A85 L03 U11 U14 V04 W01 W04 X12
IN HARAZONO, M; HAYASHI, K; HORI, M; IINO, Y; SASAMORI, R; SHIKADA, H
PA (KYOC) KYOCERA CORP
CYC 2
PI JP 2000165052 A 20000616 (200059)* 9p
US 6207259 B1 20010327 (200119)
ADT JP 2000165052 A JP 1998-339376 19981130; US 6207259 B1 US 1999-428824 19991028
PRAI JP 1998-339376 19981130; JP 1998-311643 19981102; JP 1999-217011 19990730
AB JP2000165052 A UPAB: 20011012

NOVELTY - A multi-interconnection layer structure (B), formed by insulating layers (1) containing thermosetting resin at concentration less than 20 ppm, is arranged over a core wiring board (A), so that difference between the thermal expansion coefficients of wiring board and the multi layer structure is equal to predefined value. The thickness of the multi layer structure is, B at most 2/3 of the core wiring board (A).

DETAILED DESCRIPTION - A **wiring circuit layer** (2) formed by embedding a metallic foil under the surface of the insulating layer (1), is connected to the core wiring board through the via-hole **conductors** (3). The difference between the **glass transition** temperature of the thermosetting resin provided in the core wiring board and the insulating layer is less than 30 deg. C.

USE - For portable telephone, video camera.

ADVANTAGE - Prevents disconnection or short circuit of wiring board. Prevents curvature or bending of substrate. Reduces manufacturing cost and time by forming **wiring circuit layer** and insulating layer, simultaneously.

DESCRIPTION OF DRAWING(S) - The drawing indicates a sectional view of multi **layer wiring** board.

Insulating layer 1
Wiring circuit layer 2
Via-hole **conductors** 3
Core wiring board A
Multi layer structure B

Dwg.1/4

L46 ANSWER 8 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2000-421941 [36] WPIX

DNN N2000-314800 DNC C2000-127540
TI Ball grid array package for integrated circuits includes wire-**bonding sites** connected to tape-layer contact area and connector for connecting tape-layer contact area to circuit board contact area.
DC A85 L03 U11
IN HAMZEHDOOST, A
PA (VLSI-N) VLSI TECHNOLOGY INC
CYC 1
PI US 6069407 A 20000530 (200036)* 6p
ADT US 6069407 A US 1998-195349 19981118
PRAI US 1998-195349 19981118
AB US 6069407 A UPAB: 20000801
NOVELTY - A die-up ball grid array package (200), includes rigid circuit board (202) whose surfaces are connected by **conductors**, flexible insulated-tape layer (240) and integrated-circuit die (204). Wire-**bonding sites** (250) are connected to tape-layer contact areas (260a,260b) on (240). Tape-layer contact areas (260a,260b) are connected to circuit board contact area on (202) by a connector.

DETAILED DESCRIPTION - A ball grid array (BGA) package comprises (i) rigid circuit board (202) whose top and bottom surfaces are connected by plurality of electrical **conductors**. The electrical **conductor** has circuit board contact areas at the top surface of the rigid circuit board; (ii) flexible insulated-tape layer (240) which has upper surface (242) and lower surface (244), fixed to the upper surface of the rigid circuit board. (242) has a number of wire-**bonding sites** (250) and (244) has a number of tape-layer contact areas (260a,260b); and (iii) integrated-circuit die (204) having a pair of opposing surface, a die-mounting bottom surface (206) and top surface (208) which has wire-bonding pads (210). (206) of the integrated-circuit die is mounted to upper surface of flexible insulated-tape **layer**. The **wire-bonding sites** (250) on the upper surface of flexible insulated-tape layer are electrically connected to respective contact areas (260a,260b). The bonding-wire loops (252), connect wire-bonding pads formed on the integrated-circuit die to respective wire-**bonding sites** on the upper surface of flexible insulated-tape layer. The respective tape-layer contact areas (260a,260b) are connected to the circuit-board contact area of the electrical **conductor**. A plurality of solder balls (280a,280b) are connected to the lower surface of the rigid circuit board (202) and to the **conductors** formed through the rigid circuit board. A sealing unit (290) for covering and sealing the integrated-circuit die and bonding wires.

USE - For integrated circuit.

ADVANTAGE - The BGA package combines an insulated-tape **layer** with **circuit** board, thereby reducing cost. Large openings are not required through the insulated-tape layer to allow the solder balls to extend through the openings, to contact the areas on insulated tape layer top surface. The routing of conductive traces on the insulated tape-layer top surface is easy. The existing via fabrication techniques is used to form vias in the insulated tape **layer**. The **circuit** boards have only vias and no etched **conductors**, hence can be produced economically.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of encapsulated die-up BGA package.

Die-up BGA package 200
Rigid printed board 202
Integrated-circuit die 204
Die-mounting bottom surface 206
Top surface 208
Wire-bonding pads 210

Vias 220
Plated-through holes 222,270
Flexible insulated tape layer 240
Upper surface 242
Lower surface 244
Wire-**bonding sites** 250
Bonding-wire loops 252
Contact areas 260a,b
Via 262
Conductive traces 268
Solder balls 280a,b
Adhesive material 282
Sealing part 290
Dwg.2/2

L46 ANSWER 9 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2000-356206 [31] WPIX
DNN N2000-267310
TI Wiring board for mounting hybrid integrated circuits, optical components, includes laminated **circuit wiring layer** comprising metallic **conductor** layer, non-formation area in which electronic component is connected.
DC V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 2000114685 A 20000421 (200031)* 5p
ADT JP 2000114685 A JP 1998-285366 19981007
PRAI JP 1998-285366 19981007
AB JP2000114685 A UPAB: 20000630
NOVELTY - A laminated **circuit wiring layer** (2) is formed on **insulated base** (1). The **wiring layer** comprises sequentially arranged cementing layer (3), barrier layer (4) and main metallic **conductor** layer (5). Electronic component (A) is connected in the area (7) where the metallic **conductor** layer is not formed via wax material (6).
USE - For mounting hybrid ICs, optical components such as optical isolator, lens, optical fiber, etc. Also for mounting active and passive components such as semiconductor device, capacitor, resistors, etc.
ADVANTAGE - **Circuit wiring layer** can be formed with high density, since the **wiring layer** is formed on **insulated base** by thin film coating technology, thus miniaturization of **wiring layer** is attained.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of wiring board.
Insulated base 1
Wiring layer 2
Cementing layer 3
Barrier layer 4
Metallic **conductor** layer 5
Wax material 6
Area 7
Dwg.1/1

L46 ANSWER 10 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 2000-166541 [15] WPIX
DNN N2000-125036
TI Connection pad mounting structure of surface mounting type ceramic wiring board e.g. BGA package - has insulated substrate on whose base, connection pads are mounted with diameter set based on pitch of adjacent pad and specific relation is maintained between total area of connection pads and

pad formation area.
DC U11
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 2000022017 A 20000121 (200015)* 7p
ADT JP 2000022017 A JP 1998-188940 19980703
PRAI JP 1998-188940 19980703
AB JP2000022017 A UPAB: 20000323
NOVELTY - Connection pads (5) are formed at the base of an insulated substrate. Connecting terminals (6) made of wax material are connected to the connection pad. The diameter of these pads is 55-65% of the pitch of adjacent connection pad. The total area of all the connection pads is 20% or more than the connection pad formation area. DETAILED DESCRIPTION - A **wiring circuit layer** made of low resistance metal is formed on an insulated substrate made of crystallized glass. **Wiring layer** (8) is formed on the **insulated base** (7) of an external circuit board (B). Connection pads formed at the base of the insulated substrate of the ceramic wiring board (A) are connected to the **wiring layers** through connecting terminals. An INDEPENDENT CLAIM is also included for ceramic wiring board mounting structure.

USE - For surface mounting type ceramic wiring board e.g. ceramic package such as BGA package.

ADVANTAGE - The ceramic wiring board is mounted firmly on an external circuit board made of glass **epoxy resin**. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the ceramic wiring board mounting structure. (5) Connection pad; (6) Connecting terminal; (7) **Insulated base**; (8) **Wiring layer**; (A) Ceramic wiring board; (B) External circuit board.
Dwg.1/4

L46 ANSWER 11 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-597113 [51] WPIX
DNN N1999-441390 DNC C1999-174223
TI Adhesive for multiwire wiring board - comprises siloxane modified polyamidoimide resin and thermosetting component.
DC A85 L03 V04
PA (HITB) HITACHI CHEM CO LTD
CYC 1
PI JP 11261240 A 19990924 (199951)* 8p
ADT JP 11261240 A JP 1998-56291 19980309
PRAI JP 1998-56291 19980309
AB JP 11261240 A UPAB: 19991207
NOVELTY - The adhesive comprises siloxane modified polyamidoimide resin and thermosetting component. The softening temperature of the adhesive (at B stage) is 20-100 deg. C and has a coefficient of linear expansion below 1000 ppm/ deg. C at a **glass transition** temperature of 170-350 deg. C. The storage modulus of the adhesive is 30 MPa or more at 300 deg. C.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacture of multiwire wiring board which involves either application of adhesive agent on the insulated substrate (1) or transfer of the carrier film containing adhesive agent to the insulated substrate. An insulated **coating wire** (5) is fixed on the substrate containing adhesive layer (4), which is then heat pressed for hardening of the adhesive. A hole (7) is drilled through the substrate and its inner wall is plated to form **conductor** circuit (2).

USE - The adhesive is used for multiwire wiring board which consists of an insulated **substrate, conductor circuit**, adhesive **layer**, insulated **coating wire** and through hole (10) (claimed).

ADVANTAGE - The adhesive for multiwire wiring board has an excellent property to suppress or reduce the insulation resistance and to position the insulated **coating wire** accurately. The adhesive excels in flexibility and skin layer formation. The solvent in the adhesive is removed at low temperature in a short time.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional drawing of multiwire wiring board manufacturing process. (1) Insulated substrate; ; (2) Conducted circuit; ; (3) Under lay layer; ; (4) Adhesive layer; ; (5) Insulated **coating wire**; ; (7) Hole; ; (8) Surface circuit; ; (10) Through hole.

Dwg.1/1

L46 ANSWER 12 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-410609 [35] WPIX
DNN N1999-306971 DNC C1999-121365
TI Wiring board for mounting large scale integrated circuit element - has magnetic material that consists of sintered compact, formed on periphery of through holes in **insulated base**.
DC L03 U11 V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 11163221 A 19990618 (199935)* 6p
ADT JP 11163221 A JP 1997-326796 19971127
PRAI JP 1997-326796 19971127
AB JP 11163221 A UPAB: 19991011

NOVELTY - The magnetic material that consists of sintered compact is formed on periphery of the through holes (3) in the **insulated base** (1). The sintered compact includes filler component that consists of quartz and any one of cristobalite, tridymite, enstatite and forsterite in range of 20-80 volume%. The **wiring layers** (2) are filled in the through holes.

DETAILED DESCRIPTION - The upper connection pad (2a) and the lower connection pad (2b) are formed at extending ends of the **wiring layers** on top and bottom surface of the base. The upper connection pad is connected to the electrode of the semiconductor chip (4) and the lower connection pad is connected to the wiring **conductor** (5a) of the external **circuit substrate** (5). The base is made of lithium oxide of 5-30 wt% and lithium silica glass of 20-80 vol% with melting point of 400-800 deg. C.

USE - For mounting large scale integrated circuit element.

ADVANTAGE - Absorbs noise in **wiring layer** by converting it to heat energy. Maintains normal operating state of chip without influence of noise. Prevents attenuation of electric signal. Avoids loss of magnetism of magnetic material by reducing calcination temperature of base.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of wiring board. (1) **Insulated base**; (2) **Wiring layer**; (2a) Upper connection pad; (2b) Lower connection pad; (3) Through hole; (4) Semiconductor chip; (5) External **circuit substrate**; (5a) Wiring **conductor**.

Dwg.1/1

L46 ANSWER 13 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-273887 [23] WPIX
DNN N1999-205445
TI Insulated resin layer of printed circuit used for portable personal computer, portable telephone and video camera - includes insulated resin layer which is formed between **conductor** metal of through-hole and base material of printed circuit.
DC V04
PA (HITA) HITACHI LTD

CYC 1
PI JP 11087869 A 19990330 (199923)* 6p
ADT JP 11087869 A JP 1997-245006 19970910
PRAI JP 1997-245006 19970910
AB JP 11087869 A UPAB: 19990630
NOVELTY - Insulated resin layer (6) is formed between the **conductor** metal of a through-hole (7) and the resin **insulated base** material of printed circuit. The resin **insulated base** material contains glass fiber. Resin of the insulated resin layer is different from that of the resin **insulation base** material. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for manufacturing method of printed circuit.
USE - In printed circuit used for portable personal computer, portable telephone and video camera.
ADVANTAGE - The resin **insulated base** material is made to form between the **conductor** metal of a through-hole so that the printed circuit has high reliable insulation. An inexpensive thing is used as resin so the insulation reliability and the through-hole durability is enhanced. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the manufacturing process of printed circuit. (1) Glass fiber; (4) Inside **layer wiring**; (5) Hole; (7) Through-hole; (9) Outer **layer wiring**.
Dwg.1/3

L46 ANSWER 14 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-127698 [11] WPIX
DNN N1999-093878
TI Wiring board for hybrid integrated circuit - includes thin **film wiring conductor layer** made of nickel- chrome and internal **wiring layer** which are made to contact each other by interposing metal layer.
DC U11 V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 11004077 A 19990106 (199911)* 5p
ADT JP 11004077 A JP 1997-156421 19970613
PRAI JP 1997-156421 19970613
AB JP 11004077 A UPAB: 19990324
NOVELTY - An internal **wiring conductor layer** (2) made of copper is formed on the surface of a crystallised glass sintered **insulated base** (1). A thin **film wiring conductor layer** (3) made of nickel-chrome and the internal **wiring layer** are made to contact each other by interposing a metal layer (4).
USE - For hybrid integrated circuit.
ADVANTAGE - Forms entire **wiring conductor layer** with high density. Large attenuation is not given to electrical signal which propagates internal **wiring conductor layer** if internal **wiring conductor layer** is formed with copper. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of wiring board. (1) **Insulated base**; (2) Internal **wiring conductor layer**; (3) Thin **film wiring conductor layer**; (4) Metal layer.
Dwg.1/1

L46 ANSWER 15 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-119809 [10] WPIX
CR 1998-158807 [14]; 1998-321561 [28]; 1998-387048 [33]; 1998-413095 [35]; 1998-426977 [36]; 1998-494730 [42]; 1999-141884 [12]; 1999-166601 [14]; 1999-403948 [34]; 1999-467829 [39]; 1999-525955 [44]; 2000-513923 [46];

2000-523631 [47]; 2000-564465 [52]; 2002-597688 [64]
DNN N1999-087460 DNC C1999-034843
TI Forming resin-impregnated cloth with less pinholes for manufacturing printed circuit boards - by coating fibres of cloth with first thermosetting resin initially without filling interstices and coating cloth with a second resin which fills its interstices after partially curing the first resin..
DC A85 L03 P73 V04
IN APPELT, B K; JAPP, R M; PAPATHOMAS, K; RUDIK, W J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5858461 A 19990112 (199910)* 8p
ADT US 5858461 A Div ex US 1996-716815 19960910, US 1997-891629 19970709
FDT US 5858461 A Div ex US 5719090
PRAI US 1996-716815 19960910; US 1997-891629 19970709
AB US 5858461 A UPAB: 20021010
Core is made from at least one sheet of cloth (10), having fibres with interstices between them, by coating and surrounding the fibres with a selected thermosetting resin (14) while leaving essentially all of the interstices unfilled and coating a second selected thermosetting resin over the first, essentially to fill all the interstices unfilled by the first coating, after curing the first coating sufficiently beyond B-stage cure so that it will not dissolve in the **uncured resin** of the second coating. The second coating is subsequently B-stage cured to obtain a smooth, essentially continuous, cross-linked polymer, transition zone between the two coatings and the sheet is laminated between two metal sheets by applying heat and pressure, essentially sufficient to cure fully the resins impregnating the cloth and largely eliminate pin hole defects.
USE - Method is used to form resin-impregnated fibreglass sheets for manufacturing printed circuit boards.
ADVANTAGES - Method results in a resin-impregnated cloth having a significantly reduced pin hole density so that there is less likelihood of a short developing between adjacent power planes or power and ground planes which are separated by the cloth. Consequently, the resin-impregnated cloth can be made using a less expensive, thicker, coarser weave cloth.
Dwg.1/8

L46 ANSWER 16 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1999-046251 [04] WPIX
CR 1999-046252 [04]
DNN N1999-033750
TI Multilayer printed wiring board and interstitial via hole manufacturing method - using laser beam for holes, etching metallic layer, forming projecting conductors on surfaces of via holes, adhesive layers for second circuit board, **uncured resin** and laminating boards together.
DC A85 L03 V04
IN ENOMOTO, R; HIRAMATSU, Y
PA (IBIG) IBIDEN CO LTD
CYC 23
PI WO 9856219 A1 19981210 (199904)* JA 33p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN KR SG US
JP 11054926 A 19990226 (199919) 13p
JP 11054934 A 19990226 (199919) 13p
EP 1009204 A1 20000614 (200033) EN
R: DE FI FR GB SE
ADT WO 9856219 A1 WO 1998-JP2497 19980605; JP 11054926 A JP 1998-172192 19980604; JP 11054934 A JP 1998-172191 19980604; EP 1009204 A1 EP 1998-923140 19980605, WO 1998-JP2497 19980605

FDT EP 1009204 A1 Based on WO 9856219
PRAI JP 1997-165291 19970606
AB WO 9856219 A UPAB: 20000712
Holes (40a) are formed with a laser beam through an insulating substrate (40) on which a metallic layer (42) is formed. After the holes are formed, via holes (36a) are formed by filling up the holes with a metal (46) and a conductor circuit (32a) is formed by etching the metallic layer. Then, a single-sided circuit board (30A) is formed by forming projecting conductors (38a) on the surfaces of the via holes.

The projecting conductors of the circuit board are put on the conductor circuit (32b) of another single-sided circuit board (30B) with adhesive layers (50) composed of an **uncured resin** in between and heated and pressed against the circuit (32b). The projecting conductors get in the **uncured resin** by pushing aside the resin and are electrically connected to the circuit. Since single-sided circuit boards (30A,30B,30C,30D) can be inspected for defective parts before the boards are laminated upon another, only defectless single-sided circuit boards can be used in the step of lamination.
Dwg.1/9

L46 ANSWER 17 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1998-068454 [07] WPIX
DNN N1998-054262
TI Manufacturing method of suspension with circuit wiring for magnetic head used in magnetic disk unit - involves forming protective **layer** on **circuit** wiring pattern of base layer after which elastic metal layer is subjected to predefined process to obtain suspension of desired shape.
DC T03
IN INABA, M
PA (NIMF) NIPPON MEKTRON KK
CYC 2
PI JP 09306114 A 19971128 (199807)* 5p
US 5809634 A 19980922 (199845)
ADT JP 09306114 A JP 1996-118998 19960514; US 5809634 A US 1997-848831 19970505
PRAI JP 1996-118998 19960514
AB JP 09306114 A UPAB: 19980223
The method involves forming an **electrically conductive** layer on a board-shaped flexible **insulated base** layer (2). The base layer along with a metal layer of elastic nature constitutes a laminated sheet. A mask is applied on predefined part of **electrically conductive** layer of laminated sheet, after which photo etching process is carried out.

The base layer is etched to suitable thickness and required circuit wiring pattern (3) is formed. A protective layer (4) is formed on the circuit wiring pattern. Finally, the elastic metal layer is subjected to photo etching and predefined processing to obtain a suspension (1) of desired shape.

ADVANTAGE - Improves operativity.
Dwg.1/4

L46 ANSWER 18 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1997-500625 [46] WPIX
DNN N1997-417319 DNC C1997-159157
TI Wiring board for hybrid DC appts - has first-second circuit part directly connected to intermediate metal layer formed on wiring **conductor**
.
DC L03 U14 V04
PA (KYOC) KYOCERA CORP

CYC 1
PI JP 09237947 A 19970909 (199746)* 8p
ADT JP 09237947 A JP 1996-42529 19960229
PRAI JP 1996-42529 19960229
AB JP 09237947 A UPAB: 19971119
The board has an **insulated base** (3) on surface, which is provided with W. A circuit **conductor** made from Cu is formed on the outside surface of the **insulated base**. A wiring **conductor** (2) made from Mo, nickel and cobalt is formed suitably in the **insulated base**. An intermediate metal layer (4) is formed directly on the wiring **conductor** formed on the surface of the **insulated base**.

The intermediate metal layer is made from W, Mo and boron alloys. A first **circuit layer** (5) covers the intermediate metal layer. 0.5-5.0wt of CuO, 0.5-2.0wt of glass and 1.0-5.0wt of W are compositions contained in the first **circuit layer**. A second **circuit layer** (6) covers the first **circuit layer**.

ADVANTAGE - Improves adhesive strength. Obtains electric conduction.
Dwg.1/2

L46 ANSWER 19 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1997-074960 [07] WPIX
DNN N1997-062360 DNC C1997-024119
TI Printed circuit board - has conductive **circuit layer**, **wire circuit layer**, insulating **coating wires**, insulation **layer** and connection holes.
DC G03 L03 V04
IN ARIKE, S; SHINADA, E; SUZUKI, T; TSURU, Y
PA (HITB) HITACHI CHEM CO LTD
CYC 2
PI JP 08321681 A 19961203 (199707)* 9p
US 5928757 A 19990727 (199936)
US 6042685 A 20000328 (200023)
ADT JP 08321681 A JP 1995-128102 19950526; US 5928757 A US 1996-653468 19960524; US 6042685 A Div ex US 1996-653468 19960524, US 1998-192213 19981116
FDT US 6042685 A Div ex US 5928757
PRAI JP 1995-128102 19950526
AB JP 08321681 A UPAB: 19970212
PCB consists of a **conductor circuit layer**, a **wire circuit layer** in which insulating **coating wires** are fixed to an adhesive layer, an insulating layer, and connecting holes provided at locations required for connection. The **conductor circuit layer** is insulated from the other circuit **conductors**. A difference in **glass transition** pt. between the adhesive layer and the adjoining insulating layer is within 60deg.C. Also claimed is prodn. of the multi-wired circuit board comprising: (a) providing the adhesive layer on the **conductor circuit layer** insulated by the insulating layer, or at least one surface of the insulating **layer**; (b) **wiring** the insulating **coating wires** on the adhesive layer for fixing; (c) providing the insulating layer on the wiring; (d) providing the connecting holes at the locations required for connection. A difference in **glass transition** pt. between the adhesive layer and the adjoining insulating layer is within 60 deg.C.

ADVANTAGE - Difference in **glass transition** pt. between the adhesive layer and the adjoining insulating layer of within 60deg.C evolves no high stress generating peeling or voids. The multi-wired circuit board has depressed peeling and voids. The multi-wired

board enables high density and high multilayer formation.
Dwg.0/4

L46 ANSWER 20 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1996-495322 [49] WPIX
DNN N1996-417826
TI Installation **circuit substrate** for multichip module, multilayer interconnection PCB - has fifth **electrically conductive** layer which has hardness higher than that of copper, is provided on fourth **electrically conductive** layer.
DC U11 V04
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 08255977 A 19961001 (199649)* 11p
ADT JP 08255977 A JP 1995-56961 19950316
PRAI JP 1995-56961 19950316
AB JP 08255977 A UPAB: 19961205
The substrate has a first **electrically conductive** layer (2) of hardness higher than that of copper formed on an organic **insulator base** layer (1). A second **electrically conductive** layer (4) of hardness higher than that of copper is sandwitched between third and fourth conductive layers (3,5) of hardness lower than that of Ni.

A fifth **electrically conductive** layer (6) of hardness higher than that of copper is provided on the fourth conductive layer.

USE/ADVANTAGE - For semiconductor device installation. Improves connection intensity, crack proof nature. Improves reliability during examination of substrate.
Dwg.2/6

L46 ANSWER 21 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1996-347857 [35] WPIX
DNN N1996-293145
TI Multi-**layer** printed **wiring** board for e.g. mounting electric component - has **conductor** circuit and dummy ground with no pattern connection that are set up at space less than 0.5 mm from connection ground or from other dummy grounds.
DC V04
PA (IBIG) IBIDEN CO LTD
CYC 1
PI JP 08162765 A 19960621 (199635)* 5p
ADT JP 08162765 A JP 1994-306439 19941209
PRAI JP 1994-306439 19941209
AB JP 08162765 A UPAB: 19960905
The board (100) has a **conductor circuit** (20) **layered** through an **insulated base** material (40). The **conductor** circuit is connected in pattern to several connection grounds. A through hole (30) is formed between each connection ground (21), and is connected electrically between the layers of the **conductor** circuit.

The **conductor** circuit and a dummy ground (22) with no pattern connection are set up at a space of less than 0.5 mm from the connection ground or from other dummy grounds.

ADVANTAGE - Reduces generation of barrel crack from heat impulse due to presence of dummy ground. Provides highly-reliable multilayer printed wiring board of through hole according to simple structure.
Dwg.1/7

L46 ANSWER 22 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1996-347670 [35] WPIX

CR 1996-347656 [35]; 1996-347666 [35]
DNN N1996-292958
TI Semiconductor device mounting structure e.g LSI - has terminal with bulb like projection part which is attached to connection pad which adheres to recess set up at lower surface of **insulated base**..
DC U11
IN ITO, N; MATSUDA, S
PA (KYOC) KYOCERA CORP
CYC 2
PI JP 08162565 A 19960621 (199635)* 5p
US 6225700 B1 20010501 (200126)
ADT JP 08162565 A JP 1994-304719 19941208; US 6225700 B1 US 1995-567949 19951206
PRAI JP 1994-304719 19941208; JP 1994-304718 19941208; JP 1994-304720 19941208
AB JP 08162565 A UPAB: 20020626
The mounting structure consists of a wiring electric **conductor** (8) which is formed on an external electric **circuit substrate** (B). A semiconductor device which accommodates a semiconductor element in a receptacle is mounted on the substrate. The receptacle comprises an **insulated base** (1) and a cover.

A metallized **wiring layer** (3) is formed on the lower surface of the **insulated base**. A connection pad (3a) adheres to a recess (1b) set up at the lower surface of the **insulated base**. A terminal (4) comprises bulb like projection part (4a) which is formed between the electric **conductor** and the connection pad. The metallised **wiring layer** is connected to the connection pad electrically.

ADVANTAGE - Prevents exfoliation of connection pad from **insulated base** by thermal stress. Carries out firm electric connection of each electrode of semiconductor IC element to external circuit.

Dwg.2/2

L46 ANSWER 23 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1995-124998 [17] WPIX
DNN N1995-098935 DNC C1995-056864
TI Printed circuit board having resin impregnated fibre sheet substrate - with through-holes filled with conductive paste in contact with metal foils forming electrical circuits on the substrate surface.
DC A85 L03 V04
IN HATAKEYAMA, A; KAWAKITA, K; KOJIMA, T; NAKATANI, S; OGAWA, T; SOGOU, H
PA (MATU) MATSUSHITA ELECTRIC IND CO LTD; (MATU) MATSUSHITA ELEC IND CO LTD; (MATU) MATSUSHITA DENKI SANGYO KK; (HATA-I) HATAKEYAMA A; (KAWA-I) KAWAKITA K; (KOJI-I) KOJIMA T; (NAKA-I) NAKATANI S; (OGAW-I) OGAWA T; (SOGO-I) SOGOU H
CYC 6
PI EP 645951 A1 19950329 (199517)* EN 39p
R: DE FR GB
JP 07170046 A 19950704 (199535) 19p
CN 1106188 A 19950802 (199730)
EP 645951 B1 19980812 (199836) EN
R: DE FR GB
DE 69412405 E 19980917 (199843)
US 5972482 A 19991026 (199952)
US 6211487 B1 20010403 (200120)
US 2001002294 A1 20010531 (200131)
US 6326694 B1 20011204 (200203)
ADT EP 645951 A1 EP 1994-114885 19940921; JP 07170046 A JP 1994-194004 19940818; CN 1106188 A CN 1994-116432 19940919; EP 645951 B1 EP

1994-114885 19940921; DE 69412405 E DE 1994-612405 19940921, EP 1994-114885 19940921; US 5972482 A Cont of US 1994-309735 19940921, Cont of US 1996-607249 19960304, US 1996-740261 19961025; US 6211487 B1 Cont of US 1994-309735 19940921, Cont of US 1996-607249 19960304, Div ex US 1996-740261 19961025, US 1999-379008 19990823; US 2001002294 A1 Cont of US 1994-309735 19940921, Cont of US 1996-607249 19960304, Div ex US 1996-740261 19961025, Div ex US 1999-379008 19990823, US 2000-741001 20001221; US 6326694 B1 Cont of US 1994-309735 19940921, Cont of US 1996-607249 19960304, Div ex US 1996-740261 19961025, US 1999-337407 19990621

FDT DE 69412405 E Based on EP 645951; US 6211487 B1 Div ex US 5972482; US 2001002294 A1 Div ex US 5972482, Div ex US 6211487; US 6326694 B1 Div ex US 5972482

PRAI JP 1993-236220 19930922; JP 1993-262175 19931020

AB EP 645951 A UPAB: 19950508
Printed circuit board has resin impregnated fibre sheet substrate (101) with at least one through-hole (103a) which is filled with conductive resin cpd. (103) for electrical connection, substrate and conductive resin cpd. being bonded together.

Also claimed is mfr. of a printed circuit board by laminating cover films to both sides of an **uncured resin** impregnated fibre sheet substrate having voids, forming at least one through-hole (103a) in the substrate using a laser, filling the hole or holes with conductive paste (103), removing the cover films and applying metal foil (102) to at least one side of the substrate, bonding the substrate and conductive paste using heat and pressure, and forming predetermined patterns on the metal foil.

ADVANTAGE - Printed circuit board has higher reliability because of the improved adhesion between the conductive resin cpd. and the walls of through holes.

Dwg.1/14

L46 ANSWER 24 OF 43 WPIX (C) 2003 THOMSON DERWENT

AN 1993-258927 [32] WPIX

DNN N1993-199173

TI Flexible multilayer circuit wiring board - has circuit **conductors** forming finger lead-like terminals made of material with high Young's modulus, and flexible wiring **conductors** on other side of **insulating base.**

DC U11

IN INABA, M; IWAYAMA, T; MIYAGAWA, A

PA (NIMF) NIPPON MEKTRON KK

CYC 3

PI WO 9315520 A1 19930805 (199332)* JA 10p
W: DE US
JP 05206589 A 19930813 (199337)
US 5408052 A 19950418 (199521) 5p
JP 3330387 B2 20020930 (200271) 3p

ADT WO 9315520 A1 WO 1993-JP29 19930112; JP 05206589 A JP 1992-34489 19920124; US 5408052 A WO 1993-JP29 19930112, US 1993-117150 19930913; JP 3330387 B2 JP 1992-34489 19920124

FDT US 5408052 A Based on WO 9315520; JP 3330387 B2 Previous Publ. JP 05206589

PRAI JP 1992-34489 19920124

AB WO 9315520 A UPAB: 19931118
The flexible multilayer circuit wiring board has, on one end of one side of a flexible **insulation base** material (1), circuit **conductors** (2) which are for forming finger lead-like terminals (3), and made of a conductive metal having a high Young's modulus.

On the other side of the flexible **insulation base** material (1) inclusive of a bent part (A) of the circuit wiring board, provided is a required circuit wiring **conductor** (4) made of a

conductive metal having a high flexibility. A through-hole (5) is provided by which the circuit **conductors** (2) and the required parts of the circuit **conductor** (4) are electrically connected to each other.

ADVANTAGE - Finger-like terminals are hard to deform even when forming finer circuit **conductors** protruded in form of finger leads whose bent part is sufficiently flexible.

Dwg.1/3

L46 ANSWER 25 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1993-193454 [24] WPIX
DNN N1993-148445 DNC C1993-086342
TI Curved circuit plate prodn. - involves laminating substrate and **uncured resin** impregnated base material, pressing, heating and moulding in mould having curved pressure surface.
DC A32 A85 L03 P73 V04
PA (MATW) MATSUSHITA ELECTRIC WORKS LTD
CYC 1
PI JP 05121872 A 19930518 (199324)* 4p
ADT JP 05121872 A JP 1991-278121 19911024
PRAI JP 1991-278121 19911024
AB JP 05121872 A UPAB: 19931116
A curved circuit comprises a resin-impregnated base material, and a circuit formed on the surface of the resin-impregnated **circuit.** A **substrate** is formed such that resin of the resin-impregnated base material is cured sufficiently to have no fluidity on subsequent moulding process. An **uncured resin**-impregnated base material is formed such that resin is fluidised on subsequent process and an adhesion is provided. The substrate and the **uncured resin**-impregnated base material are laminated together, and the laminate is pressurised, heated, and moulded by a mould the pressure surface of which is curved.

USE/ADVANTAGE - Since formation of a circuit is simply completed before processing of a curved surface, a circuit is formed without using conduction paste and there is no need for difficult curved surface printing in which conduction paste and a resist material are printed on a curved surface.

base

Dwg.1/3

Dwg.1/3

L46 ANSWER 26 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1993-082390 [10] WPIX
DNN N1993-063029 DNC C1993-036977
TI Binder for circuit plate having good coating property - comprises acid- or oxidn. agent-soluble cured heat resistant resin powder dispersed in **uncured** heat resistant **resin** matrix which becomes insol. after curing.
DC A21 A85 L03 V04
PA (IBIG) IBIDEN CO LTD
CYC 1
PI JP 05029760 A 19930205 (199310)* 13p
JP 2834912 B2 19981214 (199904) 12p
ADT JP 05029760 A JP 1991-205616 19910723; JP 2834912 B2 JP 1991-205616 19910723
FDT JP 2834912 B2 Previous Publ. JP 05029760
PRAI JP 1991-205616 19910723
AB JP 05029760 A UPAB: 19931025
Binder comprises (a) a cured heat resistant resin powder soluble to an acid or an oxidn. agent dispersed into (b) an uncured heat resistant type resin matrix which becomes insol. in acid or oxidn. agent after curing.

Solid content concn. in (a), (b) and a curing agent is 55-85%.

Prepn. of a print circuit plate pref. comprises coating the binder on a substrate by roll coater, curing, surface-roughening using an acid or an oxidn. agent, then electroless plating, etc..

ADVANTAGE - The binder has improved coating property

Dwg.0/0

L46 ANSWER 27 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1991-217327 [30] WPIX
DNN N1991-165875
TI Forming insulating layer on printed circuit board - using photo-setting dry film resist curable by ultraviolet light, with jumper wire formed on layer.
DC V04
IN HARUYAMA, S; KAWAKAMI, S; OKONOGI, H
PA (NICM-N) NIPPON CMK CORP
CYC 4
PI GB 2240221 A 19910724 (199130)*
JP 03196691 A 19910828 (199141)
US 5234745 A 19930810 (199333) 4p
GB 2240221 B 19940330 (199410) 2p
ADT GB 2240221 A GB 1990-27821 19901221; JP 03196691 A JP 1989-337196 19891226; US 5234745 A US 1990-606553 19901031; GB 2240221 B GB 1990-27821 19901221
PRAI JP 1989-337196 19891226
AB GB 2240221 A UPAB: 19930928

A base material plate (10) for the printed circuit board is provided before forming a circuit pattern (12,14) on the plate. An insulating layer (20) is provided on the circuit pattern and a conducting circuit (18) on the insulating layer.

The insulating layer is a photo setting dry film resist curable by UV light. The circuit forms a jumper wire crossing over the **conductors** (12). After exposure of the ultra violet light, the whole surface of the printed circuit board is rinsed in a solvent to remove the unnecessary portion and to leave a required film layer.

ADVANTAGE - Manufacture of multi **layer** printed **circuit** board avoids need for troublesome conducting inspection because no faulty printed circuit boards arise. @(5pp Dwg.No.1/1)@

L46 ANSWER 28 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1990-309519 [41] WPIX
DNN N1990-237667 DNC C1990-133755
TI Bonding type heat-resistant laminate sheet - comprises heat-resistant **resin** film, **uncured** phenol oxy ether polymer layer and release sheet.
DC A28 A85 A94 L03 P73 U11
PA (FUJO) FUJIMORI IND CO LTD; (TNEN) TONEN SEKIYU KAGAKU KK
CYC 1
PI JP 02219636 A 19900903 (199041)* 6p
JP 2784453 B2 19980806 (199836) 6p
ADT JP 02219636 A JP 1989-41406 19890221; JP 2784453 B2 JP 1989-41406 19890221
FDT JP 2784453 B2 Previous Publ. JP 02219636
PRAI JP 1989-41406 19890221
AB JP 02219636 A UPAB: 19930928

A bonding type heating-resistant laminate sheet has a layer structure which is composed of a heat resistant resin film layer (1)/ a uncured phenoloxyether type crosslinking polymer layer (2)/ a release sheet (3).

The heat resistant resin film layer (1) is a film of poly(parabanic aicd) type resin, poly(ether ether ketone) type resin, poly(ether sulphone) type resin, or polyester type resin.

Prodn. of the bonding type heat resistant laminate sheet involves

coating a resin liq. contg. the phenoxyether type polymer and a crosslinking agent onto the release sheet (3) or the heat resistant resin film layer (1), drying, and laminating the film layer (1) or the release sheet (3), respectively and correspondingly.

USE/ADVANTAGE - For the cover-lay films and base films of flexible printed **circuit** boards, **films** for the tape automated bonding, etc. For use, the release paper is removed, and the phenoxyether layer (2) having tacky adhesive properties, is bonded to a Cu foil, a Cu pattern-formed surface, a Cu wire, an Al foil, etc. The poly(parabanic acid) layer as the heat resistant film layer (1) is superior in heat resistant and electric insulation properties.

1/1

L46 ANSWER 29 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1990-028372 [04] WPIX
DNN N1990-021626 DNC C1990-012583
TI Radiation cured **substrate** for **circuit** cards - is made from highly filled UV light or electron beam curable resin.
DC A85 L03 V04
PA (ANON) ANONYMOUS
CYC 1
PI RD 308054 A 19891210 (199004)*
ADT RD 308054 A RD 1989- 19891120
PRAI RD 1989- 19891120; RD 1989-308054 19891120
AB RD 308054 A UPAB: 19930928
Substrate is made using a highly filled UV- light or Electron Beam curable resin.

The filler package is a blend of reinforcing and non-reinforcing fillers. Glass fibres and mica or glass fibres and glass beads are used. The **uncured resins** are low mol. wt., low viscosity liquids.

USE/ADVANTAGE - They can be filled to high levels (more than 70%) to give properties important to surface mount technology, e.g. low thermal expansion, high stiffness and high temp. resistance. The resins can be partially cured in stages during mfg. The substrate can be cured to a relatively low hardness to allow insertion of components and connectors and then fully cured. The stickiness of the surface is controlled to allow adhesion of foils or platable inks. Soft, semi-cured substrate are embossed with circuit patterns and topographical features.

0/0

L46 ANSWER 30 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1985-283568 [46] WPIX
DNN N1985-211294 DNC C1985-122804
TI Circuit with polymer film contg. electroconductive structure - pref. formed by carbonisation with electron or laser radiation.
DC A85 L03 U11 V04
IN BERNDT, K; DUNSCH, L; GERBER, D
PA (UYDR) UNIV DRESDEN TECH
CYC 1
PI DD 161232 A 19850731 (198546)* 7p
ADT DD 161232 A DD 1980-233434 19800821
PRAI DD 1980-223434 19800821; DD 1980-233434 19800821
AB DD 161232 A UPAB: 19930925
Circuit, e.g. a PC or IC element, has polymer coating(s) rendered electroconductive, in which electroconductor traces, structures and/or terminals are structurised.

The conductor trace includes a raised contact surface. A thin film of **uncured** phenolic **resin**, e.g. novolak, treated with a crosslinker, e.g. hexamethylene tetramine, pref. dissolved in alcohol, is applied to the substrate by spraying or other means, cured and

structurised electrically with high energy radiation, e.g. electrons or/and a laser beam.

USE/ADVANTAGE - The circuit can be produced economically, since mfr. is simple and materials costs are reduced.

1/2

L46 ANSWER 31 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1979-88282B [49] WPIX
TI Copper foil laminate prodn. for printed **circuits** - by **coating** sheet with unsatd. polyester resin then applying foil to **uncured resin.**
DC A23 A85 L03 P73 V04
PA (MATU) MATSUSHITA ELEC IND CO LTD
CYC 1
PI JP 54138083 A 19791026 (197949)*
JP 58024268 B 19830520 (198324)
PRAI JP 1978-47016 19780419
AB JP 54138083 A UPAB: 19930901
Resin compsn. is coated on a surface of core sheet of glass fibre cloth or aromatic polyamide fibre textile, and then a Cu foil is laminated on the non-cured resin coated surface of the core sheet. The resin compsn. consists of 100 pts.wt. of unsatd. polyester resin, >=3 pts.wt. of vinyl-phenol, diene polymer having hydroxyl terminal gp. and/or polyolefin having hydroxyl terminal gp. and an appropriate amt. of isocyanate cpd..

The unsatd. polyester resin is produced by reacting an unsatd. polybasic acid (e.g. anhydrous maleic acid or anhydrous fumaric acid) with a polyhydric alcohol (e.g. ethyleneglycol or propyleneglycol). The isocyanate cpd. is toluene-dissocyanate, diphenyl.methane-dissocyanate or prepolymer of trimethylolpropane and toluene-diisocyanate.

Printed circuit fed with 100 V current can be fitted on the copper foil laminated plate.

L46 ANSWER 32 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1973-19019U [14] WPIX
TI Multilayer printed circuit mfr - in which the boards are initially coated with **uncured resin.**
DC A85 P73 V04
PA (GENE) GENERAL ELECTRIC CO
CYC 1
PI GB 1312714 A (197314)*
PRAI GB 1970-16941 19700409
AB GB 1312714 A UPAB: 19930831
At least some of the circuit boards to be assembled to form the multilayer **circuit** are **coated** with an encapsulating or bonding resin such as epoxy resin, and positioned in the required order to form an open stack which is evacuated in an evacuating enclosure and then compressed while evacuated. Collapsible layers and resin coated spacers may be disposed between the boards. The method prevents air and moisture being entrapped between the boards.

L46 ANSWER 33 OF 43 WPIX (C) 2003 THOMSON DERWENT
AN 1972-42944T [27] WPIX
TI Laminated, metallised plastic panels - with oxidised aluminium surface film etched to leave pin holes to anchor deposited.
DC A21 A32 A85 M13
PA (PEST) PERSTORP AB
CYC 3
PI DE 2162056 A (197227)*
JP 47012591 A (197227)
FR 2118115 A (197246)
PRAI GB 1970-59944 19701217

AB DE 2162056 A UPAB: 19930831
Printed **circuits substrate** laminates are pref. made of several layers of glass fibre or paper satud. with an epoxy **resin** . The dried, **uncured** laminate panels are coated with a film of oxidised Al, by oxidising an Al coating which forms acicular crystals. The crystals penetrate into the surface and on etching away from NaOH or HCl leave holes in the plastic, which remain on curing and serve to anchor a Cu film deposited by known methods.

L46 ANSWER 34 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 2002-171030 JAPIO
TI WIRING BOARD AND MANUFACTURING METHOD
IN HAYASHI KATSURA; KOGA KAZUNORI
PA KYOCERA CORP
PI JP 2002171030 A 20020614 Heisei
AI JP 2000-364762 (JP2000364762 Heisei) 20001130
PRAI JP 2000-364762 20001130
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
AB PROBLEM TO BE SOLVED: To provide a wiring board with advantages in small size, small thickness, highly minute pattern, and adaptation for all shape of electronic equipment, such as a portable information terminal or a mobile computer while high rigidity is realized even when the wiring board is small in thickness.
SOLUTION: In a wiring board 15, a **wiring circuit layer** 3 is formed in the surface and/or the inside of an insulating substrate 2 containing thermosetting **resin** in an **uncured** or semi-cured state, and at the same time, there is a via hole **conductor** 4 made up of conductive paste in the via hole in the inside of the insulating substrate 2. The wiring substrate 15 is put between dies 17a and 17b with an uneven or three-dimensional formation structure is provided and heated under pressure, so that the thermosetting type resin is made to harden completely. As a result, a wiring board having an uneven part 5, made up of a projected part 5a on one front side and a recessed part 5b the other front side or a three-dimensional formation structure with a curved face or a bent part, can be obtained.
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L46 ANSWER 35 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 2001-339164 JAPIO
TI WIRING BOARD INCORPORATING CAPACITOR ELEMENT
IN IWACHI HIROMI; IINO YUJI; HAYASHI KATSURA
PA KYOCERA CORP
PI JP 2001339164 A 20011207 Heisei
AI JP 2000-160749 (JP2000160749 Heisei) 20000530
PRAI JP 2000-160749 20000530
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a wiring board incorporating a capacitor in which high connection reliability is ensured between the wiring board and a circuit even when it is subjected to a severe heat cycle.
SOLUTION: A capacitor element 4 is placed in an air gap part 11 of a wiring board comprising an insulation board formed by laminating a plurality of insulation sheets 1, 6, 7 containing a thermosetting resin, e.g. PPE (polyphenylene ether) resin, a **wiring circuit layer** 3 formed in the insulation board and on the surface thereof, and via hole **conductors** 2. Electrodes 6 of the capacitor element 4 are connected with the via hole **conductors** 2 and the capacitor element 4 is coated, except the electrodes 6 thereof, with at least one kind of thermosetting resin 5 selected from a group of polyester resin having a **glass transition** point of 100°C or below, polyamide based resin and polyurethane based resin.
COPYRIGHT: (C)2001,JPO

L46 ANSWER 36 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1999-312868 JAPIO
TI MULTILAYER WIRING BOARD WITH BUILT-IN ELEMENT AND ITS MANUFACTURE
IN HAYASHI KATSURA
PA KYOCERA CORP
PI JP 11312868 A 19991109 Heisei
AI JP 1998-118214 (JP10118214 Heisei) 19980428
PRAI JP 1998-118214 19980428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a multilayer wiring board with built-in element which can be reduced in size and improved in element packaging density, and a method for manufacturing the wiring board.
SOLUTION: After forming a plurality of insulating layers 3a-3d containing an **uncured** thermosetting **resin**, on which **wiring circuit layers** 2 composed of via hole **conductors** 1 formed by filling up via holes with metal powder and/or metal foil, etc., are formed, a resin film 5 which has a **glass-transition** temperature higher than that the thermosetting resin contained in the insulating layers 3a-3d has and is mounted with such an electric element 8 as the tape carrier package, etc., is put between each insulating layers 3a-3d and is unified with the adjacent insulating layers. Then the laminated body is heated to the curing temperature of the thermosetting resin.
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L46 ANSWER 37 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1999-284345 JAPIO
TI CERAMIC MULTI-**LAYER WIRING** BOARD
IN YAMAMOTO SENTARO
PA KYOCERA CORP
PI JP 11284345 A 19991015 Heisei
AI JP 1998-86376 (JP10086376 Heisei) 19980331
PRAI JP 1998-86376 19980331
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a ceramic multi-**layer wiring** board with improved adhesive strength at a surface **conductor** and good insulation between surface **conductors**
.
SOLUTION: A multi-**layer circuit** board includes an **insulating base** board 10 made up of insulating layers 1a to 1g, and a surface **conductor** 4 exposed on a surface 10a of the **insulating base** board 10. The surface **conductor** 4 is buried in the **insulating base** board 10 in a way that a projected amount of the surface **conductor** 4 from the surface 10a of the insulating **conductor** 4 is 20% or below of the total film thickness (t) of the surface **conductor** 4. In this case, an exposed face 4a of the surface **conductor** 4 exposed on the face 10a of the **insulating base** board 10 is preferably made flush with the face 10a of the **insulating base** board 10.
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L46 ANSWER 38 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1999-261242 JAPIO
TI MULTI-**LAYER** PRINTED **WIRING** BOARD AND MANUFACTURE THEREOF
IN SHINADA NAGATOSHI; TSURU YOSHIYUKI; NANAUMI KEN; TAKEUCHI KAZUMASA
PA HITACHI CHEM CO LTD
PI JP 11261242 A 19990924 Heisei
AI JP 1998-61837 (JP10061837 Heisei) 19980313

PRAI JP 1998-61837 19980313
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a multi-**layer** printed **wiring** board, together with a method for manufacturing it efficiently, which is, regardless of presence of via hole, easy for higher-density and more-minute wiring, possible for thinner-film of a wiring board, comprising high heat-resistance characteristics and connection reliability.
SOLUTION: An insulating layer laminated for bonding between inner-**layer circuit** boards 1 and 1 and/or the inner-**layer circuit** board 1 and an outer-layer copper foil 3, or, an insulating layer where a via hole connecting electrically at least a **conductor** circuit formed at an adjoining insulating layer is of a heat-resistant resin composition comprising siloxane modified polyamide imide resin and thermo-setting component, and related to a setting substance of heat- resistant resin composition, **glass transition** temperature is 170°C or above, linear expansion factor at **glass transition** temperature-350°C is 1000 ppm/°C or less, and stored elastic modulus at 300°C is 30 Mpa or above.
COPYRIGHT: (C)1999,JPO

L46 ANSWER 39 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1999-261229 JAPIO
TI MANUFACTURE OF MULTI-**LAYER** PRINTED **WIRING** BOARD
IN NARISAWA HIROSHI
PA HITACHI CHEM CO LTD
PI JP 11261229 A 19990924 Heisei
AI JP 1998-56286 (JP10056286 Heisei) 19980309
PRAI JP 1998-56286 19980309
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a method for manufacturing a multi-**layer** printed **wiring** board excellent in suppressing warp or deflection.
SOLUTION: With a printed wiring board comprising at least two or more layers of **conductor circuit layers** and a via hole for connecting at least two layers of **conductor circuit layers** provided, a metal foil is placed over at least the printed wiring board comprising the **circuit layer** and an outer most layer, which are bonded for multi-layer through a prepreg. Here, plurality of printed wiring boards of **glass transition** temperature difference 10°C or less, while difference in board thickness is 0.06 mm or less, are used.
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L46 ANSWER 40 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1994-291249 JAPIO
TI MULTI-CHIP SEMICONDUCTOR DEVICE
IN TANAKA SATOSHI; TSUKAMOTO TAKETO; OFUSA TOSHIO; SEKINE HIDEKATSU
PA TOPPAN PRINTING CO LTD
PI JP 06291249 A 19941018 Heisei
AI JP 1993-98652 (JP05098652 Heisei) 19930331
PRAI JP 1993-98652 19930331
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To enable a **conductor** pattern and semiconductor chip main bodies to dissipate heat so as to enhance a multi-chip semiconductor device in heat dissipating efficiency by a method wherein a heat dissipating metal piece is provided onto a **conductor** pattern, and leads are fixed to a metal plate through the intermediary of an insulating layer.
CONSTITUTION: A metal plate 1, an **insulating base** 2,

and a **wiring circuit layer** 3 are successively laminated to form a wiring circuit board, a semiconductor mounting wiring board is composed of the wiring circuit board and a lead 4 connected to the terminal 3a of the **wiring circuit layer** 3, and semiconductor chips 5 are mounted on the semiconductor mounting wiring board. The lead 4 is directly fixed to the metal plate 1 through the intermediary of an insulating adhesive layer 7. Furthermore, a heat dissipating metal piece 8 is directly fixed to the **wiring circuit layer** 3. The heat dissipating metal piece 8 dissipates heat released from the **wiring circuit layer** 3 and the semiconductor chip 5. By this setup, heat can be transmitted from the metal board 1 to the lead 4, so that a semiconductor device can be enhanced in heat dissipating properties as a whole.

L46 ANSWER 41 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1993-145009 JAPIO
TI PACKAGE FOR ACCOMMODATING SEMICONDUCTOR ELEMENT
IN MIYAWAKI KIYOSHIGE; SAKAMOTO TATSUUMI
PA KYOCERA CORP
PI JP 05145009 A 19930611 Heisei
AI JP 1991-301759 (JP03301759 Heisei) 19911118
PRAI JP 1991-301759 19911118
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1993
AB PURPOSE: To obtain a package for accommodating a semiconductor element which package can miniaturize a data processing equipment, by forming a part of an outer electric circuit on the upper surface of a lid body. CONSTITUTION: An **insulating base** body 1 is composed of electric insulator, and has a semiconductor element mounting part A of a recessed type in the nearly central part on the upper surface. A semiconductor element 4 is fixed via adhesive agent such as resin glass and solder material. On the **insulating base** body 1, a metallized **wiring layer** 5 which is composed of high melting point metal powder and led out from the periphery of the semiconductor element mounting part A to the bottom surface is formed. Each electrode of a semiconductor element is connected, via a bonding wire 6, with the peripheral part of the layer 5. An outer lead terminal 7 is fixed to the bottom surface via solder material. A part of the metallized **wiring layer** 5 is led out on the upper surface of the **insulating base** body 1, and connected with a metallized **conductor** layer 9 of a lid body 2. Thereby the area of an outside electric **circuit substrate** can be reduced, and a data processing equipment can be miniaturized.

L46 ANSWER 42 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1992-293298 JAPIO
TI THICK **FILM** MULTILAYER **CIRCUIT SUBSTRATE**
IN EZAKI SHIRO
PA TOSHIBA LIGHTING & TECHNOL CORP
PI JP 04293298 A 19921016 Heisei
AI JP 1991-58859 (JP03058859 Heisei) 19910322
PRAI JP 1991-58859 19910322
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1992
AB PURPOSE: To satisfactorily solder and to prevent a decrease in insulation between **conductor** wirings due to repetition of heating at the time of manufacturing. CONSTITUTION: Many **conductor wiring layers** formed of one or more gold **conductor wiring layers** 12 formed on an **insulating base**

material 11 and copper **conductor wiring layers** 14 formed on the layers 12 are laminated.

L46 ANSWER 43 OF 43 JAPIO COPYRIGHT 2003 JPO
AN 1990-117195 JAPIO
TI FORMATION SOLDER RESIST **LAYER** OF **CIRCUIT SUBSTRATE**
IN KOBAYASHI KENZO
PA FURUKAWA ELECTRIC CO LTD:THE
PI JP 02117195 A 19900501 Heisei
AI JP 1988-269553 (JP63269553 Showa) 19881027
PRAI JP 1988-269553 19881027
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1990
AB PURPOSE: To enable forming a solder resist layer without producing an undercut by forming a thick film solder resist layer by repetition of processes of forming a thin film solder resist layer and then forming a photosetting liquid resin thin layer thereon and processing to form another thin film solder resist layer.
CONSTITUTION: Ultraviolet rays are selectively applied with an ultraviolet laser 14 only to the part, where a solder resist layer is to be formed, of a thin layer 11a for selective hardening to form a thin solder resist layer 15. After hardening, a supporting plate 13 is submerged a little and another photosetting liquid resin thin layer 11a is formed on the thin solder resist layer 15. Ultraviolet rays are selectively applied from the ultraviolet laser 14 to the thin layer 11a to selectively harden said thin layer 11a into the same pattern as the solder resist layer 15. The thin solder resist layers 15 are laminated to the required thickness on a **circuit substrate** 12 by repeating these processes, the **circuit substrate** is drawn up from photosetting liquid **resin** 11, and **uncured** liquid **resin** is washed out to form a solder resist layer of the required thickness.

L47 ANSWER 3 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 2001-127160 [14] WPIX
DNN N2001-093868 DNC C2001-037202
TI Thin **film wiring** board for portable telephones, has linear **wiring layer** and reverse stand-shaped **wiring layer** of suitable thickness sequentially formed on **insulated base**.
DC L03 U11 U14 V04 W01 W02
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 2000277523 A 20001006 (200114)* 6p
ADT JP 2000277523 A JP 1999-86442 19990329
PRAI JP 1999-86442 19990329
AB JP2000277523 A UPAB: 20010312
NOVELTY - A linear **wiring layer** (3) and a reverse stand-shaped **wiring layer** (4) are sequentially formed as a circuit wiring (2) on an **insulated base** (1) selectively. The width of the linear **wiring layer** is smaller than that of the width of reverse stand-shaped **wiring layer**.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the thin **film wiring** board manufacturing method.
USE - For portable telephone and satellite communication.
ADVANTAGE - High density thin **film circuit wiring** is obtained by forming reverse stand and linear **wiring layers**. Size of apparatus is reduced by using reverse stand-shaped **wiring layer**. Reverse stand-shaped **wiring layer** reduces force impressed to **insulated base** and linear **wiring layer** . Presence of metallic material in **wiring layer** avoids peeling from **insulated base**.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of thin **film wiring** board.
Insulated base 1
Circuit wiring 2
Linear **wiring layer** 3
Reverse stand **wiring layer** 4
Dwg.1/2

L47 ANSWER 4 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1999-435912 [37] WPIX
DNN N1999-325232 DNC C1999-128362
TI Semiconductor device package structure for accommodating LSI - includes insulating layers formed below base, with oxide(s) of silicon, aluminium, magnesium, zinc, boron where lowest insulating layer contains magnetic material.
DC L03 U11
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 11176990 A 19990702 (199937)* 6p
ADT JP 11176990 A JP 1997-339084 19971209
PRAI JP 1997-339084 19971209
AB JP 11176990 A UPAB: 19990914
NOVELTY - Insulating layers (4-6) are formed below an **insulating base** (1). The lowest insulating layer (4) contains 50-90 wt.% magnetic material.
DETAILED DESCRIPTION - The **insulated base** has **wiring layers** (8) drawn from a semiconductor device mounting part (1a). A cover (2) which is attached to the **insulated base**, seals the semiconductor device mounted to the upper surface

of the mounting part.

INORGANIC CHEMISTRY - Insulating layers formed below **insulating base** are formed with SiO2-Al2O3-MgO-ZnO-B2O3 group crystallinity glass.

USE - For accommodating LSI.

ADVANTAGE - Prevents noise from seeping into a semiconductor device from an external electric **circuit substrate** and thus malfunctioning of the device, by converting noise into heat energy and absorbing. Prevents damage to the **insulated base** even if external force is applied.

DESCRIPTION OF DRAWING - The figure shows sectional view of semiconductor device package. (1) **Insulated base**; (1a) Semiconductor device mounting part; (2) Cover; (4-6) Insulating **layers**; (8) **Wiring layers**.

Dwg.1/1

L47 ANSWER 5 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1999-091813 [08] WPIX
DNN N1999-067758
TI Resin sealed semiconductor device - has **insulating base** layer over which several **wiring films** are formed and element correspondence portion in **film circuit**, whose back side is bonded with semiconductor device using bonding sheet.
DC U11
IN OHSAWA, K; SATO, K; SHIGETA, H
PA (SONY) SONY CORP
CYC 5
PI JP 10326795 A 19981208 (199908)* 8p
SG 68032 A1 19991019 (199950)
KR 98080823 A 19981125 (200005)
US 6054773 A 20000425 (200027)
TW 436938 A 20010528 (200172)
ADT JP 10326795 A JP 1997-185092 19970710; SG 68032 A1 SG 1998-609 19980324; KR 98080823 A KR 1998-10909 19980328; US 6054773 A US 1998-48843 19980327; TW 436938 A TW 1998-104391 19980324
PRAI JP 1997-77194 19970328
AB JP 10326795 A UPAB: 19990224

The device has an **insulating base** layer (2) over which several **wiring films** for ground connection are formed. One end of each of the **wiring films** are connected to the electrode of a semiconductor device (7), thus forming the semiconductor device side terminal and the other end of each of the **wiring films** form external terminals.

A **film circuit** consisting of an element correspondence portion (4) and an exterior extension (5) is also formed. The surface of the semiconductor device is bonded to the back side of the element correspondence portion of the **film circuit** through a bonding sheet (8) comprising of sheet layers (9,11) of buffer property provided on both sides of rigidity sheet layer (10) of stainless steel.

ADVANTAGE - Has high frequency noise resistant property. Allows performing connection process of electrode and ground connection process simultaneously. Reduces cost by reducing number of manufacturing processes involved.

Dwg.1/10

L47 ANSWER 6 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1998-368646 [32] WPIX
CR 1997-412839 [38]; 1998-039538 [04]; 1998-151456 [14]; 1998-236630 [21]; 1998-404841 [35]; 1999-067001 [06]
DNN N1998-288623

TI Wiring board mounting structure for semiconductor package - mounts wiring board in external electric **circuit substrate** by performing inductive coupling of first and second signal transmission tracks through slot hole.
DC U11 U14 W01 W02
IN FUJII, M; KITAZAWA, K; KORIYAMA, S
PA (KYOC) KYOCERA CORP
CYC 2
PI JP 10144818 A 19980529 (199832)* 6p
US 5952709 A 19990914 (199944)
ADT JP 10144818 A JP 1996-300129 19961112; US 5952709 A US 1997-884223 19970627
PRAI JP 1996-300129 19961112; JP 1995-342296 19951228; JP 1996-107139 19960426; JP 1996-169534 19960628; JP 1996-229922 19960830; JP 1996-320491 19961129
AB JP 10144818 A UPAB: 19991026
The structure includes a first signal transmission track (4) for connecting a semiconductor device (3) to a wiring board (1) surface. The first signal transmission track is formed on the surface of an **insulated base** (2). A ground layer (6) is provided inside the **insulated base**. A slot hole (5) is formed on the ground hole.

A second signal transmission track (8) in the **wiring layer** is formed on an external electric-**circuit substrate** (7) for mounting the wiring board. The wiring board is mounted in the **wiring layer** of the external electric-**circuit substrate**, by performing inductive coupling of the first signal transmission track with the second signal-transmission track through the slot hole.

ADVANTAGE - Improves mass production.

Dwg.1/5

L47 ANSWER 7 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1997-185856 [17] WPIX
DNN N1997-153369
TI Semiconductor element storing package e.g. for large scale integrated circuit element - has recess formed at inner peripheral area of under surface of **insulated base**, that is attached with external **circuit substrate** through low metallised layer.
DC U11 V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 09046036 A 19970214 (199717)* 4p
ADT JP 09046036 A JP 1995-198625 19950803
PRAI JP 1995-198625 19950803
AB JP 09046036 A UPAB: 19970424
The package has an **insulated base** (1) that has a position part (1a). A semiconductor element (3) is positioned on the upper surface of the position part. Multiple metallised **wiring layers** (5) are drawn from the peripheral part of the position part and are connected to multiple connection pads (6) provided under the **insulated base**.

A terminal (7) of the wiring part is attached with the connection pad. A recess (A) formed at the inner peripheral area of the under surface of the **insulated base** is connected with an external electric **circuit substrate** through a low metallised layer (9).

ADVANTAGE - Avoids generation of thermal stress between **insulated base** and external electric **circuit substrate** even when semiconductor element emits heat during

operation.
Dwg.1/2

L47 ANSWER 8 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1997-058376 [06] WPIX
DNN N1997-048236
TI Multilayered interconnectioned type **circuit substrate** mfg method - involves forming second through hole in insulated layer, through which one end of second **wiring layer** is connected to first **wiring layer**.
DC V04
PA (HITA) HITACHI LTD
CYC 1
PI JP 08307057 A 19961122 (199706)* 7p
ADT JP 08307057 A JP 1995-111491 19950510
PRAI JP 1995-111491 19950510
AB JP 08307057 A UPAB: 19970205
The method involves forming a first **wiring layer** on the surface of a copper laminate (1), which is formed on the surface of a glass epoxy base material (2). A second **wiring layer** (10) is then formed on the upper surface of the first **wiring layer**, through an insulating layer (16) which is formed on an **insulating base** material. The first, second **wiring layer** and the insulating layers constitute a multilayered body (4).

A first through hole (6) is formed at each layer of the multilayered body by penetration. One end of the second **wiring layer** is connected to the first **wiring layer** through a second through hole (8). A slot (15) is formed at the insulating layer and the second **wiring layer** is formed such that it surface coincides with the flat surface of the insulating layer.

ADVANTAGE - Facilitates high density wiring without reduction of reliability.
Dwg.1/5

L47 ANSWER 9 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1996-194024 [20] WPIX
DNN N1996-162637
TI Semiconductor-element containment package - has domain formed from surface of each ball-like terminal of high fusing point, with depth of 100 angstroms, enough to contain 2 % of chlorine atom.
DC U11
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 08064720 A 19960308 (199620)* 4p
JP 3301868 B2 20020715 (200253) 4p
ADT JP 08064720 A JP 1994-200744 19940825; JP 3301868 B2 JP 1994-200744 19940825
FDT JP 3301868 B2 Previous Publ. JP 08064720
PRAI JP 1994-200744 19940825
AB JP 08064720 A UPAB: 19960520
The package has an **insulated base** (1) having a mounting part (1a) on which a semiconductor element (3) is mounted. Two or more metallise **wiring layers** (5) are drawn from the periphery of the mounting part of the **insulated base**. Two or more connection pads (5a) electrically connected to the metallise **wiring layers**, are formed on the lower surface of the **insulated base**.

Each connection pad is connected to corresp. ball-like terminal (7) of high fusing point, through a low fusing point wax material (8). A domain with a depth of 100 angstroms which can contain 2 % of a chlorine

atom, is formed from the surface of each ball-like terminal.
ADVANTAGE - Controls oxidation of ball-like terminal and promotes diffusion of ball-like terminal and low fusing point wax material. Prevents damage of wax material due to thermal stress caused by difference in rate of thermal expansion of **insulated base** and external **circuit substrate**.
Dwg.1/2

L47 ANSWER 10 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1995-002721 [01] WPIX
DNN N1995-002436
TI Multi-chip semiconductor device with improved heat dissipation - has wiring circuit board contg. number of semiconductor chips, with metal substrate, **insulating base** material and **wiring circuit layer layered** one-by-one and positioning heat dissipation metal piece NoAbstract.
DC U11
PA (TOPP) TOPPAN PRINTING CO LTD
CYC 1
PI JP 06291249 A 19941018 (199501)* 5p
JP 3177934 B2 20010618 (200136) 4p
ADT JP 06291249 A JP 1993-98652 19930331; JP 3177934 B2 JP 1993-98652 19930331
FDT JP 3177934 B2 Previous Publ. JP 06291249
PRAI JP 1993-98652 19930331
AB JP 06291249 A UPAB: 19950110
Dwg.1/5

L47 ANSWER 11 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1991-298360 [41] WPIX
TI Mfg. multilayer thin **film circuit substrate** - by making inner stress of insulation **layer** and **wiring layer** uniform preventing circuit from sepg. from **insulation base** NoAbstract Dwg 1/4.
DC L03 U11 U14
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 03196695 A 19910828 (199141)*
ADT JP 03196695 A JP 1989-334583 19891226
PRAI JP 1989-334583 19891226; JP 1989-339583 19891226

L47 ANSWER 12 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1991-278913 [38] WPIX
DNN N1991-212978 DNC C1991-121144
TI Multilayer printer electronic circuit - comprises several inner layers each being insulating thin laminate of hard plastic-impregnated reinforcement material.
DC A85 L03 V04
IN MASIK, J
PA (PEST) PERSTORP AB; (POLY-N) POLYCLAD EURO AB
CYC 35
PI SE 465399 B 19910902 (199138)*
WO 9118491 A 19911128 (199150)
RW: AT BE CH DE DK ES FR GB GR IT LU NL OA SE
W: AT AU BB BG BR CA CH DE DK ES FI GB HU JP KP KR LK LU MC MG MW NL NO PL RO SD SE SU US
AU 9179706 A 19911210 (199212)
EP 528963 A1 19930303 (199309) EN 11p
R: AT BE CH DE DK ES FR GB GR IT LI LU NL SE
JP 05507388 W 19931021 (199347) 4p
US 5336353 A 19940809 (199431)# 3p
EP 528963 B1 19950927 (199543) EN 5p

R: AT BE CH DE DK ES FR GB GR IT LI LU NL SE
DE 69113456 E 19951102 (199549)
ADT SE 465399 B SE 1990-1766 19900516; EP 528963 A1 EP 1991-910236 19910417, WO 1991-SE270 19910417; JP 05507388 W JP 1991-509617 19910417, WO 1991-SE270 19910417; US 5336353 A WO 1991-SE270 19910417, US 1993-946429 19930111; EP 528963 B1 EP 1991-910236 19910417, WO 1991-SE270 19910417; DE 69113456 E DE 1991-613456 19910417, EP 1991-910236 19910417, WO 1991-SE270 19910417
FDT EP 528963 A1 Based on WO 9118491; JP 05507388 W Based on WO 9118491; US 5336353 A Based on WO 9118491; EP 528963 B1 Based on WO 9118491; DE 69113456 E Based on EP 528963, Based on WO 9118491
PRAI SE 1990-1766 19900516
AB SE 465399 B UPAB: 19930928
To produce the multi-**layer** printed **circuit**, several so-called inner layers are used, each comprising an insulating carrier of thin laminate of hard plastic-impregnated reinforcement material with a layer of metal or metal alloy on both sides. In this **layer** the **circuit** connections are formed. So-called pre-preg sheets (pre-impregnated sheets) of reinforcement material impregnated with hard plastic, in which the plastic is not completely hardened, are placed between the inner layers.

The inner layers are centred relative to one another, and are fixed in that position by being pressed together along their long sides. Energy is fed within a limited area along the two long sides, heating the plastic so that it hardens, binding all the layers together. The obtd. packet is laminated under heat and pressure with the pre-impregnated sheets, outer layer and/or sheets of metal or metal alloy.

USE - To produce a multi-**layer** printed **circuit** for electronic applications.
0/0

L47 ANSWER 13 OF 23 WPIX (C) 2003 THOMSON DERWENT
AN 1980-04108C [03] WPIX
TI Multilayered base plate mfr. for fitting circuit **wires** - by **coating** substrate with electroconductive high molecular blend coating with paste contg. polyamide and isoindole-quinazoline-di one, etc..
DC A26 A85 L03 P73 V04
PA (ALPS) ALPS ELECTRIC CO LTD
CYC 1
PI JP 54152159 A 19791130 (198003)*
JP 57016520 B 19820405 (198217)
PRAI JP 1978-59773 19780519
AB JP 54152159 A UPAB: 19930902
Electrically **insulating base** plate is coated with the first paste of electroconductive high molecular composite material consisting of a high molecular material such as polyimide and isoindoloquinazoline-dione and dispersed electroconductive granular filler such as metal or C black powder to form a first circuit pattern. this is then coated with a paste contg. polyimide and isoindoloquinazoline-dione to form an electrically insulating layer. One part of the electrically insulating layer is etched to form through-holes reaching the first circuit pattern. Finally the insulating layer is coated with the first paste material to form a circuit pattern connected with the first circuit pattern by means of the through-holes.

Specifically the polyimide and the isoindoloquinazoline-dione are one composite cpd. of formula (I): (where R1 and R2 are each aromatic gps. having a benzene ring and the area surrounded with dotted lines denotes the isoindoloquinazoline-dione structure).

Base plate is used for electrical communications systems or other electronic appliances.

L47 ANSWER 14 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 2001-352175 JAPIO
TI METHOD FOR MANUFACTURING MULTI-**LAYER** PRINTED **CIRCUIT** BOARD
IN KUDO YASUTO
PA SUMITOMO METAL MINING CO LTD
PI JP 2001352175 A 20011221 Heisei
AI JP 2000-174231 (JP2000174231 Heisei) 20000606
PRAI JP 2000-174231 20000606
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a method for manufacturing a multi-**layer** printed **wiring** board capable of inexpensively manufacturing a highly dense multi-layer board in which the resistance value of conductive resin wiring is reduced to the three times of the specific resistance value of pure silver.
SOLUTION: Plural constituting materials in which a via and wiring are formed by using conductive paste made of silver powder whose specific surface area is not less than 1.5 m2/g and resin whose heat decomposing temperature is not less than 400°C are prepared on a film-shaped **insulating base** material constituted of thermoplastic resin, whose heat decomposing temperature is not less than 400°C and non-organic packing materials. The constituting materials are positioned, laminated and thermo-compression bonded on the **insulating base** material, and this obtained laminated body is burnt at a temperature which is not less than 300°C.
COPYRIGHT: (C)2001,JPO

L47 ANSWER 15 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 2000-228572 JAPIO
TI FORMATION OF TERMINALS OF FLEXIBLE CIRCUIT BOARD
IN TANAKA HIDEAKI; EBIHARA SATOSHI
PA NIPPON MEKTRON LTD
PI JP 2000228572 A 20000815 Heisei
AI JP 1999-28337 (JP11028337 Heisei) 19990205
PRAI JP 1999-28337 19990205
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a method of forming the electrodes of a flexible circuit board, which enables the electrodes of a flexible circuit board to be appropriately exposed when forming a cover for protecting the surface of the **circuit wiring layer** of the flexible circuit board.
SOLUTION: A **circuit wiring layer** 1 of a desired pattern is formed on an **insulating base** material, and a mask 2 is formed on the electrodes of the **circuit wiring layer** 1. A cover coat layer 3 is applied to the top surface of the **circuit wiring layer** 1 to cover the surface of the mask 2 and is cured. The top surface of the cover coat layer 3 is then removed by a wet blast means to expose the surface of the mask 2 and form a cover layer 4 having a desired depth. The exposed mask 2 is then removed to form an opening 5 exposing the electrode.
COPYRIGHT: (C)2000,JPO

L47 ANSWER 16 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 2000-022017 JAPIO
TI CERAMIC WIRING SUBSTRATE AND PACKAGE STRUCTURE THEREOF
IN KOKUBU MASAYA; AZUMA MASAHIKO; YONEKURA HIDETO; NAGATA KOICHI
PA KYOCERA CORP
PI JP 2000022017 A 20000121 Heisei
AI JP 1998-188940 (JP10188940 Heisei) 19980703
PRAI JP 1998-188940 19980703

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide high reliable ceramic wiring substrate capable of sustaining firmly and stably connected state when a wiring substrate assuming a glass ceramics as an insulating substrate is packaged on an outer **circuit substrate** whereon a **wiring layer** is coat-formed on the surface of the insulating substrate containing organic resin by brazing process and the package structure thereof.
SOLUTION: In the package structure of a ceramic wiring substrate wherein a ceramic wiring substrate A provided with an insulating substrate 1 made of a glass ceramics, a **wiring circuit layer** 4 made of a low resistant metal formed on the surface or inside the insulating substrate 1 and a plurality of connecting pads 5 formed on the bottom face of the insulating substrate 1 is electrically connected to an outer **circuit substrate** B wherein **wiring layers** 8 are coat-formed on the surface of an **insulating base** substrate 7 containing organic resin between the connecting pads 5 and the **wiring layers** using the connecting terminals 6 made of spherical wax material. The pad diameter x of the connecting pads 5 is formed to be 55-65% of the intercentral distance y. Furthermore, it is recommended that the thermal expansion difference between the insulating substrate 1 and the **insulating base** substrate 7 may be 1-8 ppm/°C.
COPYRIGHT: (C)2000,JPO

L47 ANSWER 17 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1997-054788 JAPIO
TI METHOD FOR DESIGNING PRINTING CIRCUIT BOARD, PRINTING CIRCUIT BOARD AND ELECTRONIC EQUIPMENT PROVIDED WITH PRINTING CIRCUIT BOARD
IN OTAKI TORU
PA CANON INC
PI JP 09054788 A 19970225 Heisei
AI JP 1995-205513 (JP07205513 Heisei) 19950811
PRAI JP 1995-205513 19950811
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To reduce the generation of radiation noise caused mainly by a power source line when an IC having a multipin lead is mounted on a two-**layer** printing **circuit** board in place of a multilayer printing circuit board.
SOLUTION: In order to mount an electronic circuit element on the two-**layer** printer **wiring** plate 1 in which printing circuit patterns are formed on a surface 1a and a back face 1b via an **insulated base** part 100, a land 8 is arranged on the surface, a ground pattern 2 is extended up to the inside part of the electronic circuit element, the trunk power source pattern 5 of a trunk is arranged, a branching is performed from the trunk power source pattern, the branching is extended up to the inside portion of the electronic circuit element and a power source branching pattern 3 is connected to a part of the land via a throughhole 6. An inductance pattern is formed so that the inductance formed between the power source branching pattern and the trunk power source pattern may be larger than the inductance between a bypass capacitor arranged in the vicinity of the power source branching pattern and the power source branching pattern 3.
COPYRIGHT: (C)1997,JPO

L47 ANSWER 18 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1995-045963 JAPIO
TI MULTILAYER WIRING BOARD
IN TANAHASHI SHIGEO
PA KYOCERA CORP
PI JP 07045963 A 19950214 Heisei

AI JP 1993-186556 (JP05186556 Heisei) 19930729
PRAI JP 1993-186556 19930729
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1995
AB PURPOSE: To provide a multilayer wiring board in which the electric signal of a circuit interconnection can be transferred at high speed and in which, when a superconducting element such as a Josephson element or the like is connected, the high-speed drive function of the superconducting element in itself can be displayed sufficiently.
CONSTITUTION: A multilayer wiring board is formed in such a way that insulating films 2 which are composed of a polymer material and **circuit wiring films** are laminate alternately on an **insulating base** body and that the **circuit wiring films** 3 which are situated at the upper part and the lower part are connected electrically via a through hole 5 formed in the insulating films 2. The **circuit wiring films** 3 are formed of niobium, and surfaces excluding upper an lower connection regions are covered with coating layers 3a composed of aluminum.
COPYRIGHT: (C)1995,JPO

L47 ANSWER 19 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1994-216526 JAPIO
TI THIN-FILM MULTI **LAYER** PRINTED **CIRCUIT** BOARD
IN KONO CHIE
PA TOSHIBA CORP
PI JP 06216526 A 19940805 Heisei
AI JP 1993-3945 (JP05003945 Heisei) 19930113
PRAI JP 1993-3945 19930113
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To provide a thin-film multilayer printed circuit board suitable for forming a reliable multi-chip module easily, by eliminating a step part on faces of bonding pads formed in a row, and providing good conditions for bonding.
CONSTITUTION: On a main face of an **insulating base** board, a conductive **wiring layer** and an insulating layer are laminated alternately in a body, and a thin-**film** multilayer **wiring** part 2 made up of bonding pads in a row is formed at a given part of the upper face thereof. A conductive wiring in a layer provided just under a bonding pad (2f) of the thin-film multi **layer wiring** part 2 is so selected or set that the wiring width thereof becomes not less than that of the bonding pad (2f). Moreover, a dummy layer (2h) is formed in the other region under the bonding pad (2f) when there is no conductive wiring so that the face of the bonding pads in a row can be made flat.
COPYRIGHT: (C)1994,JPO&Japio

L47 ANSWER 20 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1994-164144 JAPIO
TI MULTILAYER INTERCONNECTION BOARD
IN NINOMIYA YUKIO
PA KYOCERA CORP
PI JP 06164144 A 19940610 Heisei
AI JP 1992-314988 (JP04314988 Heisei) 19921125
PRAI JP 1992-314988 19921125
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To provide a multilayer interconnection board having no bad effect on an electric signal transmitted through a metalized layer or a circuit **wiring** thin **film**, by connecting the metalized **wiring layer** on an insulating board surely with the thin-**film wiring** part.
CONSTITUTION: A multilayer interconnection board comprises an

insulating base body having a metalized **wiring layer** 5 with a connection pad 5a, and a thin-**film wiring** part made up of a **circuit wiring film** 3 alternately deposited with a high-polymer insulating film 2 that covers the **insulating base** body. The connection pad 5a of the metalized **wiring layer** and the **circuit wiring film** 3 of the thin-**film wiring** part are connected through each through holes 6 formed in the insulating film 2. The plurality of through holes 6, used for connecting the connection pad 5a of the metalized **wiring layer** and the **circuit wiring film** 3 of the thin-**film wiring** part, are formed widely in an area (B) two to one hundred times as large as a total area (A) of the connection pad 5a.
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L47 ANSWER 21 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1994-053649 JAPIO
TI WIRING BOARD
IN KONDO ISATO; TAKAMI SEIICHI
PA KYOCERA CORP
PI JP 06053649 A 19940225 Heisei
AI JP 1992-202355 (JP04202355 Heisei) 19920729
PRAI JP 1992-202355 19920729
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To realize a wiring board which enables secure and rigid electrical connection of electronic parts such as semiconductor device and a resistor or the like to a **circuit wiring film** through a connecting pad.
CONSTITUTION: In a wiring board formed by alternately stacking an insulating film 2 made of a polymer material and a **circuit wiring film** 3 on an **insulated base** material and by forming a connecting pad 5 connected with electronic parts at a part of the **circuit wiring film** 3, the **circuit wiring film** 3 has a three-layer structure formed by arranging closed contact layers 3b made of chromium or molybdenum to the upper and lower sides of a copper layer 3b and the connecting pad 5 also has a three-layer structure formed by a closed contact layer 5a made of molybdenum or chromium, a nickel sputtering layer 5b and a nickel plated layer 5c.
COPYRIGHT: (C)1994,JPO&Japio

L47 ANSWER 22 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1994-053648 JAPIO
TI WIRING BOARD
IN HAYASHI TOYOJI; IWATA YASUTOSHI
PA KYOCERA CORP
PI JP 06053648 A 19940225 Heisei
AI JP 1992-202354 (JP04202354 Heisei) 19920729
PRAI JP 1992-202354 19920729
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1994
AB PURPOSE: To realize a wiring board which can effectively prevent peeling of a connecting pad from an insulating film and enables secure and rigid electrical connection of electrical parts such as semiconductor device to a **circuit wiring film**.
CONSTITUTION: In a wiring board formed by alternately stacking an insulating film 2 made of a polymer material and **circuit wiring film** 3 on an **insulated base** material, a connecting pad 5 for connecting electronic parts is formed at a part of the **circuit wiring film** 3 and the external circumference edge A of the connecting pad 5 is covered with an

insulating film.

L47 ANSWER 23 OF 23 JAPIO COPYRIGHT 2003 JPO
AN 1989-194394 JAPIO
TI MANUFACTURE OF MULTILAYER PRINTED-WIRING BOARD
IN OUCHI TAKASHI; KAMIYAMA KOJI; KAWADA NOBUO
PA HITACHI CHEM CO LTD
PI JP 01194394 A 19890804 Heisei
AI JP 1988-18126 (JP63018126 Showa) 19880128
PRAI JP 1988-18126 19880128
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1989
AB PURPOSE: To restrict galvanic corrosion due to traveling of copper ion at high temperature, high humidity, and high voltage by performing Ni plating of an inner-**layer circuit** and a penetration hole.
CONSTITUTION: By etching a substrate wherein copper foil is laminated to an **insulation base** material 1, a copper inner-**layer circuit** 2 is provided. An inner-**layer circuit** 3 by Ni plating is formed up to a thickness of 10μm or more in the inner-**layer circuit** 2. An insulation layer 4 is provided on the front and back surfaces of the printed-circuit board, a penetration hole 5 is made, and an inner-wall surface 6 is covered with an Ni plating 8 wherein the thickness exceeds 15μm. According to this configuration, galvanic corrosion due to traveling of copper ion is restricted at high temperature, high humidity, and high voltage and a highly reliable multi-**layer** printed-**wiring** hoard can be obtained.

L52 ANSWER 4 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1997-074960 [07] WPIX
DNN N1997-062360 DNC C1997-024119
TI Printed circuit board - has conductive **circuit layer**, **wire circuit layer**, insulating **coating wires**, insulation **layer** and connection holes.
DC G03 L03 V04
IN ARIKE, S; SHINADA, E; **SUZUKI**, **T**; TSURU, Y
PA (HITB) HITACHI CHEM CO LTD
CYC 2
PI JP 08321681 A 19961203 (199707)* 9p
US 5928757 A 19990727 (199936)
US 6042685 A 20000328 (200023)
ADT JP 08321681 A JP 1995-128102 19950526; US 5928757 A US 1996-653468 19960524; US 6042685 A Div ex US 1996-653468 19960524, US 1998-192213 19981116
FDT US 6042685 A Div ex US 5928757
PRAI JP 1995-128102 19950526
AB JP 08321681 A UPAB: 19970212
PCB consists of a conductor **circuit layer**, a **wire circuit layer** in which insulating **coating wires** are fixed to an adhesive layer, an insulating layer, and connecting holes provided at locations required for connection. The conductor **circuit layer** is insulated from the other circuit conductors. A difference in glass transition pt. between the adhesive layer and the adjoining insulating layer is within 60deg.C. Also claimed is prodn. of the multi-wired circuit board comprising: (a) providing the adhesive layer on the conductor **circuit layer** insulated by the insulating layer, or at least one surface of the insulating **layer**; (b) **wiring** the insulating **coating wires** on the adhesive layer for fixing; (c) providing the insulating layer on the wiring; (d) providing the connecting holes at the locations required for connection. A difference in glass transition pt. between the adhesive layer and the adjoining insulating layer is within 60 deg.C.
ADVANTAGE - Difference in glass transition pt. between the adhesive layer and the adjoining insulating layer of within 60deg.C evolves no high stress generating peeling or voids. The multi-wired circuit board has depressed peeling and voids. The multi-wired board enables high density and high multilayer formation.
Dwg.0/4

L52 ANSWER 5 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1995-149849 [20] WPIX
DNN N1995-117561
TI Matrix type LCD device - incorporates liquid crystal driven by drive circuit installed in between two insulated substrates having matrix type arrangement of gate and drain type **wiring layers**.
DC P81 T04 U14
IN ANDO, M; KANEKO, T; MINEMURA, T; ONISAWA, K; OTA, M; **SUZUKI**, **T**
PA (HITA) HITACHI LTD
CYC 2
PI JP 07072510 A 19950317 (199520)* 6p
US 5552909 A 19960903 (199641) 9p
ADT JP 07072510 A JP 1993-221873 19930907; US 5552909 A US 1994-301202 19940906
PRAI JP 1993-221873 19930907
AB JP 07072510 A UPAB: 19950530
The matrix type LCD device carries out mutually perpendicular gate wiring and a drain wiring process on an insulated glass substrate (1). The

electrical insulation of the mutual intersection portion is carried out. A TFT is arranged near each intersection portion. The gate electrode of each TFT is connected to the gate wiring unit, while drain electrode of each transparent pixel electrode is connected to the drain wiring unit.

The substrate is covered with a layout film and a layout protection film (6). The substrate is arranged facing another transparent insulation substrate which consists of transparent electrode along with the protective film layer. The liquid crystal is placed in between the two substrates and it is driven by a liquid crystal drive **circuit**. The **film** thickness of the transparent pixel electrode is less than thickness of drain wiring portion.

ADVANTAGE - Simplifies production process of device. Reduces drain wiring resistance. Controls current leakage between gate drains. Improves performance and minimises cost of manufacture.

Dwg.1/5

L52 ANSWER 6 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1994-325924 [41] WPIX
DNN N1994-256004 DNC C1994-148216
TI **Epoxy resin** compsn. used e.g. as circuit board - contg. one of a novolak resin and an **epoxy resin**.
DC A21 A85 L03 U11 V04 W02 X12
IN NAKAMURA, H; **SUZUKI, T**; YASUDA, K
PA (MITC) MITSUI PETROCHEMICAL IND LTD; (MITA) MITSUI CHEM INC; (MITC) MITSUI PETROCHEM IND CO LTD
CYC 8
PI EP 621313 A2 19941026 (199441)* EN 11p
R: DE FR GB IT NL
CA 2121876 A 19941024 (199504)
JP 07003123 A 19950106 (199511) 8p
EP 621313 A3 19950322 (199543)
US 5677397 A 19971014 (199747)# 8p
EP 621313 B1 19980715 (199832) EN
R: DE FR GB IT NL
DE 69411618 E 19980820 (199839)
ADT EP 621313 A2 EP 1994-302908 19940422; CA 2121876 A CA 1994-2121876 19940421; JP 07003123 A JP 1994-70428 19940408; EP 621313 A3 EP 1994-302908 19940422; US 5677397 A Cont of US 1994-231304 19940422, US 1996-663375 19960613; EP 621313 B1 EP 1994-302908 19940422; DE 69411618 E DE 1994-611618 19940422, EP 1994-302908 19940422
FDT DE 69411618 E Based on EP 621313
PRAI JP 1994-70428 19940408; JP 1993-97621 19930423; US 1996-663375 19960613
AB EP 621313 A UPAB: 19941206

An epoxy compsn. comprises at least one of the following: (a) a novolak resin; and (b) an **epoxy resin**. (a) is obtd. by condensing one of formalin and paraformaldehyde with a phenol of formula (I). R1 = 4-12C alkyl; and n = 1-5. (b) is obtd. by glycidylating (a) with an epihalohydrin. Also claimed are the following: (1) a process for forming the compsn. by obtaining (a) or (b) and further curing and shaping the compsn.; and (2) a laminated prod.

USE - Laminates formed from the compsn. can be used as a **circuit substrate** in satellite communication and in the construction of printed wiring boards. The compsn. is adequate for forming copper-clad laminates and potting materials.

ADVANTAGE - The compsn. exhibits a low dielectric constant and a low dielectric dissipation factor as well as good working susceptibility after curing. Flame retardant property can be achieved by addn. of a diglycidyl ether of tetrabromobisphenol A.

Dwg.0/0

L52 ANSWER 7 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1994-111101 [14] WPIX
CR 1994-029836 [04]
DNN N1994-087034 DNC C1994-051268
TI Mfr. of multilayer printed wiring board by electroplating on resin substrate - provides improved adhesion by means of minute anchor structure formed by abrasive blasting.
DC A32 A85 L03 M11 V04
IN **NAKAMURA, T**
PA (MATU) MATSUSHITA ELEC IND CO LTD; (MATU) MATSUSHITA DENKI SANGYO KK
CYC 4
PI EP 590635 A1 19940406 (199414)* EN 20p
R: DE GB
JP 06196856 A 19940715 (199433) 11p
US 5517758 A 19960521 (199626) 13p
EP 590635 B1 19960717 (199633) EN 17p
R: DE GB
DE 69303684 E 19960822 (199639)
ADT EP 590635 A1 EP 1993-115712 19930929; JP 06196856 A JP 1993-265705 19930928; US 5517758 A US 1993-128825 19930928; EP 590635 B1 EP 1993-115712 19930929; DE 69303684 E DE 1993-603684 19930929, EP 1993-115712 19930929
FDT DE 69303684 E Based on EP 590635
PRAI JP 1992-259548 19920929; JP 1992-138361 19920529
AB EP 590635 A UPAB: 19971030
A method of plating a conductive layer on an insulating resin layer is disclosed. The surface of the insulating resin layer is dry abrasive blasted, chemically etched an the conductive layer is electroplated onto the etched surface.

Also claimed is a multilayer printed wiring board produced by the method described above. The board has conductors on the top and bottom surfaces of the substrate, insulating resin layers on the top and bottom surfaces of the substrate, through holes in desired places, second **circuit** conductor **layers** formed on the insulating resin layer and inner walls of the through holes connected to the first conductor layers via the through holes.

USE/ADVANTAGE - For mfr. of multilayer wiring board for electronic devices. The plating layer has excellent adhesion to the insulating resin **layer**. The **circuit** conductors have excellent adhesion to the insulating resin layer.

The abrasive used is aluminium or silicon carbide. The insulating resin layer is ultrasonically cleaned after dry sandblasting. The sandblasting forms irregularities with roughness of 5-12 micrometres on the surface of the insulating layer.

Dwg.1D

L52 ANSWER 8 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1993-244636 [31] WPIX
DNN N1993-188113 DNC C1993-108915
TI Novel polyimide(s) for thermosetting resins adhesives - used as insulating adhesives for bonding electronic components, as PCB bases etc..
DC A26 A81 A85 G03 L03 V04
IN IKEDA, K; IWASAKI, Y; MATSUURA, H; MIYADERA, Y; **SUZUKI, T**; TANAKA, M
PA (HITB) HITACHI CHEM CO LTD
CYC 5
PI EP 553612 A2 19930804 (199331)* EN 21p
R: DE FR GB
JP 05179141 A 19930720 (199333) 10p
JP 05186589 A 19930727 (199334) 12p
JP 05339344 A 19931221 (199404) 10p

EP 553612 A3 19931222 (199515)
US 5508357 A 19960416 (199621) 13p
US 5510425 A 19960423 (199622) 12p
EP 553612 B1 19960821 (199638) EN 22p
R: DE FR GB
DE 69304086 E 19960926 (199644)
JP 3010871 B2 20000221 (200014) 10p
JP 3144013 B2 20010307 (200116) 12p

ADT EP 553612 A2 EP 1993-100097 19930106; JP 05179141 A JP 1992-810 19920107; JP 05186589 A JP 1992-3124 19920110; JP 05339344 A JP 1992-153943 19920615; EP 553612 A3 EP 1993-100097 19930106; US 5508357 A Cont of US 1993-853 19930105, US 1994-307543 19940916; US 5510425 A Div ex US 1993-853 19930105, US 1994-270182 19940701; EP 553612 B1 EP 1993-100097 19930106; DE 69304086 E DE 1993-604086 19930106, EP 1993-100097 19930106; JP 3010871 B2 JP 1992-810 19920107; JP 3144013 B2 JP 1992-3124 19920110

FDT DE 69304086 E Based on EP 553612; JP 3010871 B2 Previous Publ. JP 05179141; JP 3144013 B2 Previous Publ. JP 05186589

PRAI JP 1992-810 19920107; JP 1992-3124 19920110; JP 1992-153943 19920615

AB EP 553612 A UPAB: 19931119
A polyimide comprising structural units (I) is new. In (I) Ar = a gp. comprising (i) 10-90 mole % of a sub-unit (a) (where n = integer 1 or more, Z = -C(O)-, -SO2-, -O-, -S-, -(CH2)m- (m = integer 1 or more), -CONH-, -C(CH3)2-, -C(CF3)2-, -C(O)O- or direct bond, one or more H on each ring opt. being substd.) and (ii) 90-10 mole % a sub-unit (b) (where R1-4 = H or 1-4C alkyl or alkoxy, at least 2 being indep. alkyl or alkoxy, and X = -CH2-, -C(CH3)2-, -O-, -SO2-, -C(O)- or -CONH-).
USE/ADVANTAGE - The novel polyimides have excellent solubility in organic solvents and low softening pt., the thermosetting compsns. permit low-temp. moulding, extrusion and forming e.g. into adhesive sheets. The cured product is heat- and solvent-resistant and the adhesive contg. **epoxy resin** can be cured at temps. as low as 180 deg.C.
Uses include insulating adhesives for bonding electronic components, as base films for (metal-clad) laminates, including flexible PCBs and multi-**layer circuit** boards, in tape automated bonding (TAB) systems in prepreg prodn., etc.
Dwg.0/2

L52 ANSWER 9 OF 11 WPIX (C) 2003 THOMSON DERWENT
AN 1990-082571 [11] WPIX
DNN N1990-063589 DNC C1990-036270
TI Applying coating between conductors of circuit pattern - by electrodepositing opaque **coating** on **circuit**, applying photocurable coating and irradiating from back of board.
DC A89 G06 L03 P81 P83
IN KAMAKURA, T; **SUZUKI, T**
PA (SHID) SHINTO PAINT CO LTD
CYC 2
PI US 4873175 A 19891010 (199011)* 4p
JP 62160421 A 19870716 (199105)
ADT US 4873175 A US 1986-947221 19861229
PRAI JP 1986-1534 19860108
AB US 4873175 A UPAB: 19930928
A functional coating film is formed on the spaces of a fine **electrically conductive** circuit pattern on a transparent base board by electrodeposition of a light-shielding coating on the circuit pattern. A photo-setting coating is applied over the entire area of the transparent base-board. The back surface of the board is exposed to light to cure portions of the photosetting coating which are not observed by the electrodeposited coating. The uncured portions of the photosetting coating, and the light shielding precoat are removed in a single process

by a reagent or solvent.
USE/ADVANTAGE - The process is used especially to fill the space between the colour stripes for a colour filter which is used in colouring a liquid crystal display.
0/0

L52 ANSWER 10 OF 11 JAPIO COPYRIGHT 2003 JPO
AN 2000-239995 JAPIO
TI INSULATING SUBSTRATE, PREPREG AND CIRCUIT BOARD PRODUCED THEREWITH
IN ECHIGO FUMIO; **KAWAKITA YOSHIHIRO**
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 2000239995 A 20000905 Heisei
AI JP 1999-41208 (JP11041208 Heisei) 19990219
PRAI JP 1999-41208 19990219
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain an insulating substrate to be impregnated with a resin varnish and suitable as a prepreg for printed board having excellent dimensional stability even under severe condition by bonding fiber-crossing points in a nonwoven fabric composed of a heat-resistant organic fiber with a binder composed of an inorganic material.
SOLUTION: A nonwoven fabric is produced by the papermaking process of an aqueous slurry of one or more heat-resistant organic fibers selected from PBO fiber, PBI fiber, para-aramid fiber, PTFE fiber and PBZ fiber, e.g. short fiber of poly-p-phenylenebenzobisoxazole(PBO). The fiber-crossing points of the nonwoven fabric are bonded with an inorganic material binder composed of a solution of a low-melting glass or an aqueous dispersion or colloidal solution of fibers or fine particles composed of a low-melting glass to obtain the objective insulating **substrate**. A **circuit** board is produced by using a prepreg obtained by impregnating the substrate with a resin varnish composed of one or more resins selected from **epoxy resin**, polyimide resin, phenolic resin and fluororesin.
COPYRIGHT: (C)2000,JPO

L52 ANSWER 11 OF 11 JAPIO COPYRIGHT 2003 JPO
AN 2000-068620 JAPIO
TI **CIRCUIT SUBSTRATE** AND MANUFACTURE THEREOF
IN NAKAYA YASUHIRO; **SUZUKI TAKESHI**
PA MATSUSHITA ELECTRIC IND CO LTD
PI JP 2000068620 A 20000303 Heisei
AI JP 1998-238580 (JP10238580 Heisei) 19980825
PRAI JP 1998-238580 19980825
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To realize a **circuit substrate** having high reliability in inner via hole connection by a method wherein at least one of interfaces of a wiring pattern with a conductive component is roughened more than an interface with an insulator layer.
SOLUTION: An interface with conductive paste 2 of a copper foil 3 laminated on an external surface of outermost insulator layers 1a, 1b of an insulator layer 1 comprising aramid nonwoven cloth with **epoxy resin** impregnated is a roughened structure. In this case, although only a connection interface of the outermost copper foil which requires land strength, similar roughening may be done also on a connection interface of an inner layer part. Especially, it may be used effectively on a sling surface of the copper foil used in the inner layer. The conductive paste 2 comprises an **epoxy resin** with copper powder mixed as a conductive composition filled in a through hole of the insulator layer 1, wherein the conductive composition may be a composition to be filled in a via hole generally, which contains metal powder such as gold and an **epoxy resin** for example as a binder.

FILE 'HCAPLUS'

L1 6309 S CIRCUIT(W)(SUBSTRATE OR LAYER? OR FILM OR COAT?)

L2 676 S INSULAT?(W)BASE

L3 18839 S (WIRING OR WIRE)(2A)(LAYER? OR FILM OR COAT?)

L4 158524 S ELECTRICAL?(W)(CONNECT? OR CONDUCTIV?)

L5 616445 S RESIN

L6 142106 S EPOXY(W)RESIN

L7 829 S THERMOSETTING(W)EPOXY(W)RESIN

L8 290 S UNCURED(W)RESIN

L9 60 S METAL(W)COHESION

E RESINS/CT

L10 300204 S RESINS+ALL/CT

E RESINS/CT

E E3+ALL/CT

L11 11967 S (RESINS/CT OR RESINIFICATION/CT OR GUM/CT OR "GUM RESINS"/CT OR "GUMS (RESINOUS)"/CT OR "NATURAL RESINS"/CT OR "RESINOUS GUMS"/CT)

L12 616450 S L5 OR L11

E EPOXY RESINS/CT

E E3+ALL/CT

L13 112128 S ("EPOXY RESINS"/CT OR "RESINS, EPOXY"/CT OR "BISPHENOL A EPOXY RESINS"/CT OR "BISPHENOL A-BASED EPOXY RESINS"/CT OR "BISPHENOL A-EPICHLOROHYDRIN EPOXY RESINS"/CT OR "CURED EPOXY RESINS"/CT OR "DIAN EPOXY RESINS"/CT OR "DIPHENYLOLMETHANE-EPICHLOROHYDRIN EPOXY RESINS"/CT OR "EPOXIDE RESINS"/CT OR "EPOXY COMPOUNDS"/CT OR "EPOXY POLYMERS"/CT OR "GLYCIDYL EPOXY RESINS"/CT OR "GLYCIDYL-CONTG. EPOXY RESINS"/CT)

L14 3 S L1 AND L7

L15 16 S L1 AND L2

L16 175 S L1 AND L3

L17 52 S L16 AND CONDUCTOR

L18 0 S L1 AND L8

L19 8 S L17 AND L4

L20 17 S L17 AND L12

L21 16226 S THERMOSETTING(W)RESIN

L22 1 S L17 AND BONDING(W)SITE

L23 0 S L17 AND TENSILE STRENGTH

L24 76 S L1 AND L21

L25 12 S L24 AND L4
L26 1 S L17 AND WALL
L27 15 S L24 AND CONDUCTOR
L28 25 S L24 AND GLASS
L29 60806 S GLASS TRANSITION
L30 1 S L24 AND L29
L31 0 S L24 AND L9
L32 11 S L24 AND L3
L33 6 S L1 AND L11
L34 553 S L1 AND L13
L35 111 S L34 AND CONDUCTOR
L36 5 S L35 AND L3
L37 37 S L35 AND L4
L38 0 S L35 AND L2
L39 11 S L24 AND L3
L40 62 S (L15 OR L19 OR L20 OR L22 OR (L25 OR L26 OR L27) OR L30 OR L32 OR L33) NOT L14
L41 54 S (L28 OR L37) NOT (L15 OR L19 OR L20 OR L22 OR (L25 OR L26 OR L27) OR L30 OR L32 OR L33 OR L14)
L42 119 S L15 OR L19 OR L20 OR L22 OR (L25 OR L26 OR L27) OR L30 OR L32 OR L33 OR L14 OR L28 OR L37
SEL PN
L43 152 S (DE2155029/PN OR DE2413158/PN OR EP734065/PN OR DE2536152/PN OR DK143289/PN OR EP12094/PN OR EP645950/PN OR EP734576/PN OR EP74605/PN OR EP768334/PN OR EP786808/PN OR EP851726/PN OR EP855720/PN OR ES2136556/PN OR ES2149699/PN OR FR2443787/PN OR JP10107445/PN OR NL175324/PN OR US6143116/PN OR AT321668/PN OR AT7404112/PN OR AU7245021/PN OR AU7247998/PN OR AU7583954/PN OR AU9852728/PN OR AU9884144/PN OR CA2187857/PN OR CH606485/PN OR CN1075338/PN OR CN1108026/PN OR CN1137324/PN OR CN1195001/PN OR CN1302179/PN OR CN1364049/PN OR DE3543924/PN OR EP1001852/PN OR EP1087261/PN OR EP1096842/PN OR EP1194025/PN OR EP1213952/PN OR FR2147337/PN OR FR2158256/PN OR FR2159848/PN OR GB1395887/PN OR GB1412986/PN OR GB1468065/PN OR GB1525012/PN OR GB1531327/PN OR HU156112/PN OR HU156458/PN OR IT961766/PN OR JP02258337/PN OR JP02281686/PN OR JP03116894/PN OR JP04001219/PN OR JP04094187/PN OR JP04169002/PN OR JP04237064/PN OR JP04372194/PN OR JP05009309/PN OR JP05082929/PN OR JP05206598/PN OR JP06013754/PN OR JP06021655/PN OR "JP06034435 B4"/PN OR JP06052715/PN OR "JP06080894 B4"/PN OR JP06122785/PN

OR JP06220368/PN OR JP06283830/PN OR "JP07034506 B4"/PN OR JP07147464/PN OR JP07173448/PN OR JP07211145/PN OR JP07226110/PN OR JP08236884/PN OR JP08259912/PN OR JP08307058/PN OR JP08330181/PN OR JP08330356/PN OR JP09046011/PN OR JP09092981/PN OR JP09232471/PN OR JP09232705/PN OR JP09246716/PN OR JP09266230/PN OR JP09324060/PN OR JP10007884/PN OR JP10051136/PN OR JP10070157/PN OR JP10178249/PN OR JP10190191/PN OR JP10208547/PN OR JP10215073/PN OR JP10335526/PN OR JP10335834/PN OR JP10335835/PN OR JP11003618/PN OR JP11003619/PN OR JP11054854/PN OR JP11054865/PN OR JP11087927/PN OR JP11097578/PN OR JP11106714/PN OR JP11224532/PN OR JP11260864/PN OR JP11260865/PN OR JP11266083/PN OR JP11298105/PN OR JP11340631/PN OR JP2000113728/PN OR JP2000138457/PN OR JP2000196240/PN OR JP2000216505/PN OR JP2000216537/PN OR JP2

L44 12 S (TOMEKAWA S OR TOMEKAWA, S OR TOMEKAWA SATORU OR TOMEKAWA, SATORU)/AU

L45 525 S (YAMASHITA, Y OR YAMASHITA Y OR YAMASHITA, YOSHIHISA OR YAMASHITA YOSHIHISA)/AU

L46 4141 S (SUZUKI TAKESHI OR SUZUKI, TAKESHI OR SUZUKI, T OR SUZUKI T)/AU

L47 75 S (KAWAKITA Y OR KAWAKITA, Y OR KAWAKITA, YOSHIHIRO OR KAWAKITA YOSHIHIRO)/AU

L48 2110 S (NAKAMURA TADASHI OR NAKAMURA TADASHI OR NAKAMURA, T OR NAKAMURA T)/AU

L49 6805 S (L44 OR L45 OR L46 OR L47 OR L48)

L50 6800 S L49 NOT L42

L51 12 S L50 AND L1

L52 261 S L50 AND ((L5 OR L6 OR L7))

L53 296 S L50 AND ((L10 OR L11 OR L12 OR L13))

L54 296 S L52 OR L53

L55 0 S L54 AND L2

L56 3 S L54 AND L3

L57 14 S L54 AND L4

L58 27 S L51 OR L56 OR L57

L59 27 DUP REMOVE L58 (0 DUPLICATES REMOVED

01/30/2003

2 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:781273 HCAPLUS
TI Process for producing a multi-**layer wiring** board
IN Hayashi, Katsura; Nishimoto, Akihiko; Hiramatsu, Yukihiro; Iino, Yuji; Tateno, Shuichi; Sasamori, Riichi; Fukumoto, Shigeaki
PA Kyocera Corporation, Japan
SO U.S., 23 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 7

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6143116	A	20001107	US 1997-937529	19970925
	JP 10107445	A2	19980424	JP 1996-254492	19960926
	JP 10178249	A2	19980630	JP 1996-338688	19961218

AB A multilayer wiring board formed by laminating a plurality of circuit board units each including an insulating board containing at least a **thermosetting resin**, and a **wiring circuit layer** formed on the surface of said insulating board, wherein said insulating board is provided with via hole conducting passages so as to **electrically connect** the **wiring circuit layers** of the neighboring circuit board units, said via hole conducting passages are formed by filling via holes formed in the insulating board with a conducting paste, and said **wiring circuit layer** is buried in the surface of the insulating board in a manner that said insulating board possesses a flat surface. The multilayer wiring board has a satisfactory flatness required for mounting flip chips. Besides, the insulating board and the via hole conducting passages are not infiltrated by chemicals such as etching solution or plating solution. There is no problem of defective circuit, and connection is highly reliably maintained offering advantage in realizing a highly dense wiring.

L40 ANSWER 27 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:779022 HCAPLUS
TI Wiring substrate and its production method. [Machine Translation].
IN Tachino, Shuichi
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000312063	A2	20001107	JP 1999-121337	19990428
PRAI	JP 1999-121337		19990428		

AB [Machine Translation of Descriptors]. When the formation it does the beer hole electric **conductor** making use of laser light in, with the incoming radiation side surface and the radiation side surface, it is not necessary the design of the wiring pattern the modification to do, offers the wiring baseplate and the production method ingredient preparation of doing the beer hole electric **conductor** whose precision is high. At least the formation it does beer hole electric **conductor** 4 A with the laminated body of plural block B1 - the B4 where longitudinal form condition consists of the raised bottom and the abbreviation trapezoid form which possesses the lower bottom as ingredient preparation it does the plural **wiring circuit layers** which the formation are done the surface of the insulated substrate and the insulated substrate which consist of the insulating material which contains the organic **resin** and / or inside, **wiring circuit layer** 3 A 2 was formed between the layer which among the **wiring circuit layers** differs and 3 B, filling up the metal powder at least inside the beer hole, being connected by the beer hole electric **conductor** 4 A which becomes, in the wiring baseplate which becomes, 2 Connect with the identical bottom side of the abbreviation trapezoid form in horn **wiring circuit layer** 3 A and 3 B beer hole electric **conductor** 4 A.

L40 ANSWER 28 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:742416 HCAPLUS
DN 133:328318
TI Multilayer printed wiring board
IN Asai, Motoo; Kariya, Takashi; Shimada, Kenichi; Segawa, Hiroshi
PA Ibiden Co., Ltd., Japan
SO PCT Int. Appl., 32 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000062588	A1	20001019	WO 1999-JP2689	19990521
	W: CN, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	JP 2000299562	A2	20001024	JP 1999-105549	19990413
	EP 1194025	A1	20020403	EP 1999-921226	19990521
	R: DE, GB, NL, FI				
PRAI	JP 1999-105549	A	19990413		
	WO 1999-JP2689	W	19990521		

AB A multilayer printed wiring board so structured that layer-to-layer **resin** insulating layers and **conductor** layers are alternately provided on a multilayer core sheet having **conductor** circuits provided on its inner layers, and a build-up **wiring layer** where **conductor** layers are connected through via holes is provided, wherein the multilayer core sheet has a **resin** insulating layer covering an inner layer **conductor** circuit provided on a core member, a via hole is made through the **resin** insulating layer and leads to the inner **conductor** circuit, through holes are made through the **resin** insulating layer and the core member and filled with a filler, and part of via holes made in a build-up **wiring layer** are positioned directly above the through holes and connected to the through holes. Even if the core sheet is a multilayer one, the **elec. connection** to the inner circuit in the core sheet through through-holes is ensured, thereby providing a multilayer printed wiring board advantageously adaptable to high d. of through holes.

L40 ANSWER 29 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:706105 HCAPLUS
TI Multilayer interconnection substrate and its production method. [Machine Translation].
IN Nishimoto, Akihiko
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000277913	A2	20001006	JP 1999-80701	19990325
PRAI	JP 1999-80701		19990325		

AB [Machine Translation of Descriptors]. As assuring the simplification of manufacturing process it is possible, when distribution facilities it does the **wiring circuit layer** which consists of the metal foil of wide area of the **wiring circuit layer** and the gland layer et cetera whose line width is wide inside the insulated substrate in, close adhesion between the **wiring circuit layer** and the insulated layer the multilayer interconnection baseplate and the production method where there is not defectiveness are obtained. At least, the **wiring circuit layer** 2 which consists of the metal foil in both sides of the insulated layer which includes the **thermosetting resin** to be buried, in order to connect the **wiring circuit layer** which at the same time was formed to both sides electrically filling up the metal powder inside the beer hole, 1st **wiring layer** 1 A, 1 C and 1 E where the beer hole electric **conductor** 3 which becomes was formed and, filling up the metal powder inside the beer hole of the insulated layer which at least includes the organic **resin** the formation doing the beer hole electric **conductor** which becomes, 2nd **wiring layer** 1 B and 1 D which become ingredient preparation do, 1st **wiring layer** 1 A, 1 C, 1 E and 2nd **wiring layer** 1 B and 1 D the laminate doing alternately, it becomes, surface roughness (Ra) of both sides of the **wiring circuit layer** in the 1st **wiring layer** is desirable in each case to be 0.2 xdmu m or more.

L40 ANSWER 30 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:687864 HCAPLUS
TI Single sided **circuit substrate**, multilayer printed board and its production method. [Machine Translation].
IN Enomoto, Akira; Karitani, Takashi
PA Ibiden Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000269647	A2	20000929	JP 1999-74432	19990318
PRAI JP 1999-74432		19990318		

AB [Machine Translation of Descriptors]. The high density multilayer printed board of IVH structure of the beer hole formation due to laser beam machining the single sided printed circuit board, the multilayer printed board and of producing that the method to at high yield rate efficiently producing of being superior in connected reliability between the ideal layer are offered. Single sided circuit baseplate 60 for the core is formed, from **insulated base** material 40 and electric conductor circuit 54 and the beer hole and padding 56. Single sided circuit baseplate 70 for the laminate - 74 is formed, from the **insulated base** material and electric conductor circuit and the beer hole and the projection condition electric conductor. The multilayer printed board the single sided circuit baseplate for the plural laminates consecutively, through the adhesive layer, vis-a-vis the single sided circuit baseplate for the core is formed the laminate after doing, by the compressed heating press of one time. At that occasion, the projection condition electric conductor of the single sided circuit baseplate for the laminate pushing away adhesive layer 58, is connected by the padding of the single sided circuit baseplate for the core, the laminate of the single sided circuit baseplate for the laminate, the projection condition electric conductor of the single sided circuit baseplate for the laminate, penetrating the adhesive layer, is connected to the electric conductor circuit of the single sided circuit baseplate for the contiguity laminate.

L40 ANSWER 31 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:581056 HCAPLUS
TI Single sided **circuit substrate** and its production method. [Machine Translation].
IN Enomoto, Akira; Karitani, Takashi
PA Ibiden Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000232268	A2	20000822	JP 1999-31019	19990209
PRAI	JP 1999-31019		19990209		

AB [Machine Translation of Descriptors]. The problematical point which accompanies the beer hole formation due to laser beam machining is cancelled, the high density multilayer printed board of IVH structure the single sided printed circuit board and its production method to at high yield rate efficiently producing of being superior in connected reliability between the ideal layer are proposed. When the electric conductor circuit which was formed to the surface of one side of the **insulated base** material and that **insulated base** material and the single sided circuit baseplate which has with the beer hole which reaches to electric conductor circuit from the other surface of the above-mentioned **insulated base** material are produced, opening for the beer hole formation, pulse energy 0.5 - 5.0 mj, pulse width 1 - 20 xdmu S, pulse interval 2 ms or more, the number of shots in origin of condition 3 - 10, must be formed the pulse oscillation type carbon dioxide gas laser - by lighting.

L40 ANSWER 32 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:533326 HCAPLUS
TI The face to face continuity method of using the face to face continuity device and the same device of the both sides **circuit substrate**. [Machine Translation].
IN Yamazaki, Takuya
PA Omron Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000216537	A2	20000804	JP 1999-11446	19990120
PRAI JP 1999-11446		19990120		

AB [Machine Translation of Descriptors]. Spare processing and the like such that continues both sides with the metal make clip is unnecessary altogether on the both sides baseplate side which is possible, to apply to also the both sides baseplate of thermoplastic **insulated base** material subject after the pattern formation, furthermore becomes object, job man-hour can be decreased. Being a device which continues between both electric conductor layer of the both sides circuit baseplate possessing the electric conductor layer in both sides of the thermoplastic **insulated base** material of sheet condition or sheet condition electrically, on side of one side of the aforementioned both sides circuit baseplate, there being on a side which is identical with the aforementioned 1st electrode component of the 1st electrode component and the aforementioned both sides circuit baseplate which possess the acute point which contact possibly is supported vis-a-vis the electric conductor layer of particular side, approaching the said 1st electrode component, the 2nd electrode component and the description above which possibly are arranged, vis-a-vis the electric conductor layer of particular side contact are supported The electric power unit in order to impress voltage between both electrode component in a state where the electrode component and the aforementioned 2nd electrode component of 1 contact the electric conductor layer, and, ingredient preparation it does.

L40 ANSWER 33 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:533310 HCAPLUS
TI Die for base material formation of **circuit substrate** and **circuit substrate**. [Machine Translation].
IN Yoshida, Hiroyuki; Nakata, Kimiaki; Kakawa, Eiji
PA Matsushita Electric Works, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000216505	A2	20000804	JP 1999-17060	19990126
PRAI JP 1999-17060		19990126		

AB [Machine Translation of Descriptors]. The circuit baseplate which productivity furthermore can be high do the circuit formation with the fine pattern without needing pattern jO process, is offered. In 3 dimension three-dimensional forms unevenness section 2 is provided on the surface of the **insulated base** material 1 which the formation is done. As the foundation electrically conducting layer 3 which, designates unevenness section 2 as boundary on the surface of **insulated base** material 1 is formed conductive material layer 4 is formed to the surface of this foundation electrically conducting layer 3. The circuit 5 which the formation is done the conductive material layer 4 which adjoins in unevenness section 2 has breaked with conductive material layer 4. As for circuit 5 the formation it is done with the unevenness section 2 which is provided in **insulated base** material 1 as contour, pattern jO process becomes unnecessary. In addition the creeping distance between circuit 5 is adjacent becomes long depending upon the unevenness section, is possible to guarantee the electric insulation hi

L40 ANSWER 34 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:475345 HCAPLUS
TI Laminate **circuit substrate**. [Machine Translation].
IN Makino, Yoichi; Sakanoe, Akihiro
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000196240	A2	20000714	JP 1998-368275	19981224
PRAI	JP 1998-368275		19981224		

AB [Machine Translation of Descriptors]. This invention is superior in continuity reliability of the internal **wiring layer** and the terminal electrode, there are times when the laminate circuit baseplate whose at the same time miniaturization is possible is offered. According to this invention, insulated layer 1 A - 1 E and internal **wiring layer** 3 the laminate doing, as on the end face of the laminated body 1 which becomes, the formation it does the concave section 51 for the terminal electrode which carries out the thickness direction of said laminated body 1, on the inner **wall** surface of concave section 51 for the aforementioned terminal electrode, connect to the **wiring layer** 3 inside the said, the inner **wall** surface of the said penetration concave section 51 which the electric **conductor** layer 52 which at the same time extends to the thickness direction of the inner **wall** surface of concave section 51 for the terminal electrode does, the exposure formation furthermore, includes said electric **conductor** layer 52 terminal electrode electric **conductor** membrane 53 the suffering wearing formation Doing, it is a laminate circuit baseplate which designates that becomes as feature.

L40 ANSWER 35 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:317733 HCAPLUS
TI Multilayer interconnection substrate and its production method. [Machine Translation].
IN Hayashi, Katsura; Hori, Masaaki
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000138457	A2	20000516	JP 1998-311643	19981102
PRAI JP 1998-311643		19981102		

AB [Machine Translation of Descriptors]. On the core baseplate surface is superior in surface even characteristic, at the same time at the little the multilayer interconnection layer offers the multilayer interconnection baseplate and the production method of being the formation possible number of processes. It consists of the insulated substrate 1 which and contains the **thermosetting resin** and the fibrous filler in appearance and the underside of the core baseplate A which possesses through hole electric **conductor** 4, the laminate doing the insulated sheet which possesses the beer hole electric **conductor** 7 where, the metal paste fills up inside the beer hole the formation it does insulated layer 6, after laminate bonding, copying the **wiring circuit layer** 8 of the copying film 9 surface on the insulated layer surface, buries the **wiring circuit layer** on the insulated layer surface, after to many layer converting process over again, heating the **thermosetting resin**, hardening completely, multilayer interconnection layer 10 of appearance side and underside side the through hole electric **conductor** of the core baseplate Connecting electrically with, obtain the multilayer interconnection baseplate B which becomes.

L40 ANSWER 36 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:610917 HCAPLUS
DN 131:229860
TI TAB-packaging adhesive tape for integrated **circuit substrates** and semiconductor devices
IN Konishi, Yukitsuna; Ogura, Mikihiro; Kikoshi, Shoji
PA Toray Industries, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11260865	A2	19990924	JP 1998-59877	19980311
PRAI	JP 1998-59877		19980311		

OS MARPAT 131:229860
AB Title adhesive tape with strong adhesion and highly elec. insulation for TAB (tape automated bonding)-packaging is fabricated by sandwiching an adhesive layer between a flexible org. insulating film and a protective film, wherein the adhesive layer comprises (a) C36 dicarboxylic acid-contg. polyamide resin, (b) .gtoreq.1 phenol deriv. represented by the formula of I (X: .gtoreq.1 S- or O-contg. group or bond; Y1, Y2: C1-5 hydrocarbyl; m: integer 0-3; n: integer 0-1), optionally (c) epoxy resin, and (d) .gtoreq.1 phenolic resin. Thus, a Lumirror [poly(ethylene terephthalate)] film-based and Upilex 75S (polyimide) film-protected adhesive tape comprising polyamide resin 100, Epikote 828 (epoxy resin) 40, CKM 1282 (phenolic resin) 40, and biphenol 40 parts, was tested showing adhesion with copper foil 1.20 kN/m (before plated) and 1.12 kN/m (after plated), adhesion retention 93%, and insulation .gtoreq. 500 h.

L40 ANSWER 37 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:610916 HCAPLUS
DN 131:229859
TI TAB-packaging adhesive tape for integrated **circuit substrates**, and semiconductor devices
IN Konishi, Yukitsuna; Ando, Yoshio; Kigoshi, Shoji
PA Toray Industries, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11260864	A2	19990924	JP 1998-58175	19980310

PRAI JP 1998-58175 19980310
OS MARPAT 131:229859
AB Title tape with strong adhesion and highly elec. insulation for TAB (tape automated bonding)-packaging is fabricated by sandwiching an adhesive layer between a flexible org. insulating film and a protective film, wherein the adhesive layer comprises (a) C36 dicarboxylic acid-contg. polyamide resin, (b) phenol deriv. represented by the formula of I (X, Y: OH, COOH, NH2, CN, SO3H; m: integer 0-2; n: integer 1-3), optionally (c) epoxy resin, and (d) .gtoreq.1 phenol resin. Thus, a Lumirror [poly(ethylene terephthalate)] film-based and Upilex 75S (polyimide) film-protected adhesive tape comprising polyamide resin 100, Epikote 828 (epoxy resin) 50, CKM 1282 (phenolic resin) 50, and 3-aminophenol 40 parts, was tested showing adhesion with copper foil 1.14 kN/m (before plated) and 1.05 kN/m (after plated), adhesion retention 92%, and insulation .gtoreq.500 h.

L40 ANSWER 38 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:231940 HCAPLUS
DN 130:312909
TI Semiconductor device and packaging of the device using adhesive film containing **thermosetting resins** and resins with low elasticity
IN Nagai, Akira; Ogino, Masahiko; Eguchi, Shuji; Segawa, Masanori; Ueno, Isao; Nishimura, Asao; Akiyama, Yukiharu; Miyazaki, Chuichi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11097578	A2	19990409	JP 1997-256420	19970922
PRAI JP 1997-256420		19970922		

AB Title device includes a tape having a **circuit layer**, a semiconductor element **elec. connected** to the tape, external terminals (for **elec. connecting** the element and a packaging substrate) on the tape, and an adhesive film comprising a **thermosetting resin** and a resin with low elasticity for bonding the tape and the element in elec. insulation. The device is manufd. by a process including (1) laminating the tape and the adhesive film, (2) laminating the adhesive film and the semiconductor element, (3) **elec. connecting** the circuit on the tape and the pad layer of the semiconductor element, (4) sealing the **elec. connection** by an elec. insulator, and (5) forming the external terminals on the tape. The adhesive film contg. elastomers with low elasticity contributes to redn. of thermal stress, i.e., takes a roll as stress buffer layer. Thus, a 80:20 mixt. of an epoxy resin and an acrylic rubber as the adhesive film was placed between a semiconductor element and a circuit tape then the laminate was pressed at 120.degree. for 30 s and cured at 170.degree. for 60 min. Then, after the pad layer of the semiconductor element and the connecting lead on the circuit tape was connected by single-point-bonding and the contact was sealed with an epoxy resin (RC 021C), solder balls (as terminals) were bonded on the tape to give title device showing no foaming in the adhesive layer after 168-h moisture absorption at 85.degree. and relative humidity 85% followed by heating at 245.degree..

L40 ANSWER 39 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:501235 HCAPLUS
DN 129:169061
TI **Electrically conductive** copper paste composition
IN Komiyatani, Toshio; Takahashi, Yoshiyuki
PA Sumitomo Bakelite Co., Ltd., Japan
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 855720	A2	19980729	EP 1998-101003	19980121
	EP 855720	A3	19990210		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 10208547	A2	19980807	JP 1997-14164	19970128
	JP 11003618	A2	19990106	JP 1997-152062	19970610
	JP 11003619	A2	19990106	JP 1997-152063	19970610
	JP 11224532	A2	19990817	JP 1998-316530	19970610
	TW 401579	B	20000811	TW 1998-87100874	19980122
	AU 9852728	A1	19980730	AU 1998-52728	19980123
	CN 1195001	A	19981007	CN 1998-106191	19980126
PRAI	JP 1997-14164	A	19970128		
	JP 1997-152062	A	19970610		
	JP 1997-152063	A	19970610		

AB In an **elec. conductive** Cu paste compn. comprising a Cu powder, a **thermosetting resin**, and a solvent as essential components, the Cu powder has a dendrite shape having an av. particle diam. of 1-25 .mu.m and a BET sp. surface area of 2000-6300 cm2/g, and the compn. imparts a high reliability and a high **elec . cond.** to the through hole portion or the like of a printed **circuit substrate**.

L40 ANSWER 40 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:466569 HCAPLUS
DN 129:116788
TI Interlaminar adhesive film for a multilayer printed wiring board, a multilayer printed wiring board using it, and production of the wiring board
IN Nakamura, Shigeo; Yokota, Tadahiko
PA Ajinomoto Co., Inc., Japan
SO Eur. Pat. Appl., 20 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 851726	A2	19980701	EP 1997-310572	19971224
	EP 851726	A3	19990707		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	TW 432907	B	20010501	TW 1997-86119686	19971224
	JP 11087927	A2	19990330	JP 1997-357420	19971225
	US 6376053	B1	20020423	US 2000-721664	20001127
PRAI	JP 1996-348448	A	19961226		
	JP 1997-168632	A	19970625		
	JP 1997-188235	A	19970714		
	US 1997-999332	B1	19971229		

AB An interlaminar adhesive film is provided for multilayer printed **wiring** boards, the **film** being attached to an internal-layer circuit board where the film is embedded in an internal-layer circuit. A process of producing a multilayer printed wiring board using the film is also provided. The adhesive film facilitates simultaneous and integral coating of an internal-layer circuit pattern and **resin** filling of through holes and/or surface via holes in a build-up process of producing a multilayer printed wiring board in which a **conductor circuit layer** and an insulation layer are alternately laminated together. The adhesive film for multilayer printed wiring boards comprises a support film base and a **resin** compn. which is solid at ambient temp., both to be laminated on an internal-layer circuit board, in which the **resin** compn. contains .gtoreq.10% by wt. of a **resin** with a lower softening point than the lamination temp. and has a thickness greater than that of the **conductor** in the internal-layer circuit; the flow of the **resin** compn. at the lamination temp. is at least of the thickness of the **conductor** of the internal-layer circuit, or is of the depth of a surface via hole if present in the internal-layer circuit, or is .gtoreq.1/2 the depth of a through hole in the internal-layer circuit singly or in combination with a surface via hole.

L40 ANSWER 41 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:250996 HCAPLUS
DN 128:329725
TI Multilayer wiring board and its production method.
IN Hayashi, Katsura; Nishimoto, Akihiko; Hiramatsu, Yukihiro
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 7

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10107445	A2	19980424	JP 1996-254492	19960926
	US 6143116	A	20001107	US 1997-937529	19970925
PRAI	JP 1996-254492	A	19960926		
	JP 1996-338688	A	19961218		
	JP 1996-350069	A	19961227		
	JP 1997-137129	A	19970527		
	JP 1997-137130	A	19970527		
	JP 1997-141759	A	19970530		
	JP 1997-206038	A	19970731		

AB A multilayer wiring board is described, which comprises insulator layers contg. at least an org. **resin layer**, **wiring circuit layers** on the insulator layers, and via-hole **conductors** for connecting the **wiring circuit layers**. The via-hole **conductors** are formed by filling via holes with a **conductor** paste, and the **wiring circuit layers** comprise metal foil formed by transferring from a transfer sheet. A method for producing the wiring board is also described. The adverse effects of etching and plating solns. on the insulator layers and via-hole **conductors** are prevented.

L40 ANSWER 42 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:154759 HCAPLUS
DN 128:277945
TI FC tapes and TAB tapes employing intrinsic polyimide base films in assembling semiconductor devices
IN Okada, Koji
PA Kanegafuchi Chemical Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10070157	A2	19980310	JP 1996-224737	19960827
PRAI	JP 1996-224737		19960827		

AB The base films laminated in FC tapes (protective/adhesive/**insulative-base** film laminates) employed in tape-automatic-bonding (TAB) for assembling semiconductor devices are made from polyimide block copolymers I (R1 = divalent org. group m; R2 = divalent org. groups selected from phenylene, biphenylene, and naphthalenediyl, unsubstituted or substituted by Me, Cl, Br, F, MeO-; R3 = tetravalent org. group; m,n are integers) which has low thermal expansion, low moisture-absorption, and low moisture-caused expansion. The semiconductor devices and circuits are patterned by laminating a Cu film and pattering the Cu film on the FC tapes after delamination of the base film by TAB process. The polyamide film provides the FC tapes in TAB processing with an expansion coeff. equiv. to that of metal and glass and with a modules of elasticity high enough in prevention of warping and curling for precision fabrication of semiconductor devices and integrated circuits.

L40 ANSWER 43 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:619401 HCAPLUS
DN 127:302212
TI Manufacture of surface laminar printed circuit containing **conductor** film showing high adhesion with insulating layer
IN Miura, Takeyuki; Kiyota, Masaru; Imanari, Masaaki; Nawafune, Hidemi
PA Learonal Japan, Inc., Japan; Nawafune, Hidemi
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09246716	A2	19970919	JP 1996-55256	19960313
PRAI	JP 1996-55256		19960313		

AB The manuf. involves the following steps; (1) prehardening, surface roughening, and completely hardening a **thermosetting resin** coated on a **circuit substrate** to give an insulating layer, (2) introducing an acidic group into the insulating layer, (3) ion exchanging the acidic group with a metal ion, (4) reducing the metal-adsorbing acidic group to convert to a **conductor** metal film, and (5) forming a Cu pattern on the metal film.

L40 ANSWER 44 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:266604 HCAPLUS
DN 126:257864
TI Glassy carbon substrate for electric circuit
IN Oota, Kojiro; Kamata, Mitsuji
PA Hitachi Chemical Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09046011	A2	19970214	JP 1995-198838	19950803
PRAI	JP 1995-198838		19950803		

AB The substrate comprises glassy carbon support with thermal cond. .gtoreq.5 W/mK, which is prepd. from a **thermosetting resin** contg. a plasticizer, and an elec. insulator layer on the face for the circuit. The substrate with high thermal cond. and low thermal expansion is manufd. from cure-molded **thermosetting resin** contg. a plasticizer by carbonizing in nonoxidn. atm. Void-free elec. insulator layer can be formed on the substrate free from pores inside as a result of addn. of the plasticizer.

L40 ANSWER 45 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:127288 HCAPLUS
DN 126:138563
TI Fabrication of multilayer printed circuits connecting interlayers by solder melting
IN Haruta, Yoichi; Matsumoto, Takeya; Kanbayashi, Tomio; Hiraoka, Hideki; Fujiwara, Masahiro
PA Toa Gosei Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08307058	A2	19961122	JP 1995-129399	19950428
PRAI	JP 1995-129399		19950428		

AB The title process involves thermally laminating a Cu-lined and base-sol. polymer insulative sheet on an internal panel, etching and base-dissolving to give the laminate blind via-holes, curing the polymer material, mounting a solder ball on the blind via-holes, and subsequently melting the solder ball to connecting between the external and internal Cu films. The process makes possible to give blind via holes by etching the Cu film and base-dissoln. of polymer, instead of drilling, and then melting solder ball.

L40 ANSWER 46 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:294800 HCAPLUS
DN 122:121108
TI Thick-film electric **circuit substrates** and their manufacture
IN Sakabe, Kenichi; Yamamoto, Taijiro
PA Asahi Chemical Ind, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06283830	A2	19941007	JP 1993-66531	19930325
	JP 3073358	B2	20000807		
PRAI	JP 1993-66531		19930325		

AB The **conductors** in the substrates have rectangular cross section of height .gtoreq.20 .mu.m and have distribution of thickness within .+-.20% of the av. thickness and the interlayer insulator comprise liq. photosensitive **resin** cured products of mol. wt. 1500-50,000 and ethylenic unsatd. bond concn. 10-2-2 .times. 10-4 mol/g and comprising prepolymers having ethylenic unsatd. bonds and ethylenic monomers. The substrates are manufd. by application of .gtoreq.20 .mu.m-thick liq. photosensitive **resin** after optional treatment with electroless plating catalysts; exposure and development of the **resin** layer for resist patterning; optional electroless plating on the **resin** -free part followed by electroplating of metals for **conductor** formation; and transferring of the formed resist pattern and the **conductor** onto insulating substrate and removal of base support for forming **conductor** wirings with insulators in between them. Densely wired thick wirings can be formed.

L40 ANSWER 47 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:193461 HCAPLUS
DN 122:83886
TI Thermosetting coating compositions for electrically insulating wires
IN Sanuki, Tetsuo; Oochi, Susumu
PA Sumitomo Durez Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06220368	A2	19940809	JP 1993-9405	19930122
PRAI	JP 1993-9405		19930122		

AB The title compns. contain 5-40% **thermosetting resins** mainly comprising dimethylene ether type phenolic resins (and epoxy resins), fillers, and additives. Thus, 940 parts PhOH was treated with 490 parts 80% paraformaldehyde to give a dimethylene ether type phenolic resin, 18 parts of which was mixed with 82 parts fused silica and 0.6 part powd. silica to give a powd. compn., which was mixed with MEK to give a coating with viscosity 27 P, which was dip coated on an alumina substrate patterned with a paste of Ag/Pd, dried, then cured at 150.degree. to give a test element having 0.6-mm film, which showed good resistance to moisture and thermal shock.

L40 ANSWER 48 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:459397 HCAPLUS
DN 121:59397
TI **Electrically conductive** thermoplastic and/or **thermosetting resin** compositions, coatings, inks, and substrates for electric circuits
IN Kato, Naoki; Fukada, Hiroyuki
PA Nikkiso Co Ltd, Japan; Nippon Achison Kk
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06122785	A2	19940506	JP 1991-326181	19911210
PRAI	JP 1991-326181		19911210		

AB The title compns. contain gas-phase grown carbon fibers, carbon black, thermoplastic resins, and/or **thermosetting resins**. Thus, vinyl chloride polymer was dissolved in MEK, then mixed with 50 parts graphite fiber (obtained from gas-phase grown carbon fiber; diam. 0.4 .mu.m, length 15 .mu.m) and 25 parts furnace black to give a coating, which was spread on a phenolic resin substrate, then dried to give a 25-.mu.m coating film showing elec. resistance 10.2 .OMEGA./sq.

L40 ANSWER 49 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:313778 HCAPLUS
DN 120:313778
TI Manufacture of multilayered **circuit substrate**
IN Kobarikawa, Takashi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06013754	A2	19940121	JP 1992-165945	19920624
PRAI	JP 1992-165945		19920624		

AB The substrate is manufd. by forming a Cu circuit pattern on an elec. **insulated base** substrate via a metal adhesive layer, oxidizing the exposed pattern to form a Cu oxide coating layer, applying a polyamic acid on the coated pattern, and curing to form a polyimide layer. Reaction between the Cu pattern and the polyimide layer was prevented.

L40 ANSWER 50 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:287884 HCAPLUS
DN 120:287884
TI Manufacture of multilayer ceramic **circuit substrate**
IN Someta, Hiroki
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06021655	A2	19940128	JP 1992-174002	19920701
PRAI JP 1992-174002		19920701		

AB The manuf. of the ceramic substrate involves filling via holes of ceramic green sheets with an **elec. conductive** powder and .gtoreq.1 metal powder, which fuses with the **elec. conductive** powder, and sintering the **elec. conductive** powder in liq. phase. The metal powder may be partially substituted with an alloy powder or a glass powder. The manuf. may involve laminating green sheets having via holes filled with the **elec. conductive** powder and a **wiring layer**, and sintering. The **elec. conductive** filler for the via holes may contain .ltoreq.24 vol.% metal or glass powder. The interlayer elec. **conductors** of the substrate have high d. and low resistance.

L40 ANSWER 51 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:50635 HCAPLUS
DN 118:50635
TI Electric conductive pastes and fabrication of multilayer ceramic electric circuit boards
IN Nakatani, Seiichi; Nishimura, Tsutomu; Juhaku, Sei; Hakotani, Yasuhiko
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04169002	A2	19920617	JP 1990-297969	19901101
PRAI	JP 1990-297969		19901101		

AB The title paste comprises (1) 90.0-99.5 wt.% powd. Au (av. particle size <10 .mu.m), (2) 0.5-10.0 wt.% powd. inorg. contg. Ni, Pt, and/or Pd (av. particle size <10 .mu.m), and (3) a solvent and an org. binder. The title fabrication of the circuit board by a glass-ceramic mixt. insulator involves (1) patterning a circuit with the above-described paste and also contacts with a CuO paste both on the insulator substrate, (2) heating to remove their solvent and binder in air, (3) reducing the patterned CuO circuit with a H-contg. reductive gas, and subsequently (4) sintering the circuit, contacts, and the substrate in a N-contg. atm. The arrangement for the Au upper **circuit layer** gives easy **wire** -bonding and soldering on the circuit.

L40 ANSWER 52 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:238853 HCAPLUS
DN 114:238853
TI Manufacture of metal-base substrate
IN Nishimoto, Yoshio
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02281686	A2	19901119	JP 1989-102738	19890421
PRAI	JP 1989-102738		19890421		

AB The title manuf. comprises laminating ceramic paper insulating layer with an **elec. conductive** metal foil, in which the foil is coated with a mixt. of 2 semi-hardened **thermosetting resins** with different setting speed. The manuf. gives the metal-base substrate with high heat releasability and high peel strength.

L40 ANSWER 53 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:229017 HCAPLUS
DN 104:229017
TI Metal core printed boards
IN Takahama, Takashi; Kitamura, Yoichi; Chijo, Hideki; Hashizume, Aiichiro
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61026288	A2	19860205	JP 1984-146762	19840717
	JP 06080894	B4	19941012		
PRAI	JP 1984-146762		19840717		

AB Metal-core printed circuit boards with a heat-resistant coating are manufd. for electronic devices. The metal core (esp. an Al strip) is coated with a water-sol. resin by electrophoresis, and overcoated with a catalyst soln. contg. .ltoreq.5% water before the resin is hardened by baking. The core with a hardened resin layer is then masked, and coated with an **elec. conductive** pattern from electroless bath.. Thus, baths with PdCl2 and SnCl2 catalysts were used to deposit a Cu pattern on circuit board resistant to heat.

L40 ANSWER 54 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1983:226558 HCAPLUS
DN 98:226558
TI Substrate for hybrid integrated circuit
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 58018997	A2	19830203	JP 1981-117440	19810727

PRAI JP 1981-117440 19810727

AB A reliable and low-cost substrate for a hybrid integrated circuit is prepd. by forming a ceramic layer (e.g., Al2O3) over a metal substrate (e.g., Al), impregnating the ceramic layer with a **thermosetting resin** (e.g., an epoxy resin), removing the surface layer of the **thermosetting resin**, and forming a **conductor** layer (e.g., Cu) with a desired pattern.

L40 ANSWER 55 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1983:208628 HCAPLUS
DN 98:208628
TI Multilayer **circuit substrate**
IN Saito, Tamio
PA Toshiba Corp., Japan
SO Eur. Pat. Appl., 18 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 74605	A2	19830323	EP 1982-108225	19820907
	EP 74605	A3	19850320		
	R: DE, FR, GB				
	JP 58044799	A2	19830315	JP 1981-143476	19810911
	JP 58093397	A2	19830603	JP 1981-192224	19811130
	JP 58093398	A2	19830603	JP 1981-192225	19811130
	US 4525383	A	19850625	US 1982-415798	19820908
PRAI	JP 1981-143476		19810911		
	JP 1981-192224		19811130		
	JP 1981-192225		19811130		

AB A multilayer **circuit substrate** having improved heat dissipation contains inorg. oxide (mainly SiO2) insulator layers and Cu **conductor** layers. An **elec. conductive** layer which can be wire bonded (Au, Ag, or Al) is formed on the uppermost Cu layer by low-temp. deposition and photoetching.

L40 ANSWER 56 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1981:184506 HCAPLUS
DN 94:184506
TI Printed wiring board
IN Shirai, Haruo; Tanaka, Yoshikatsu; Kosuga, Zinzo; Osaka, Kiyoshi
PA Shin-Kobe Electric Machinery Co., Ltd., Japan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4243474	A	19810106	US 1979-23883	19790326
	JP 54127573	A2	19791003	JP 1978-35689	19780328
PRAI	JP 1978-35689		19780328		

AB A printed wiring board with 2 **elec. conductive circuit layers** on an insulating laminate can be prepd. by using an insulating laminate with metal foils provided on both sides. A pattern is formed on 1 foil by printing and etching. Connecting through-holes are formed in the 1st insulating layer, and an **elec. conductive** member is provided in the through-holes. A 2nd insulating layer is attached to the 1st insulating layer to cover the 1st **elec. cond. circuit layer**. Then the other metal foil is patterned by printing and etching. The conductive connective through-holes can be formed by electroless metal plating, electroplating, forcing a melted solder into the holes by rolling, or forcing an **elec. conductive** paint into the holes by screen printing. The 2nd insulating layer is attached to the 1st by heating and pressurizing a multi-ply **thermosetting resin** impregnated sheet material as the 2nd insulating layers together with the 1st layer. This step may cause filling of the through-holes with insulating material of the 2nd insulating layer. The **elec. conductive** member in the through-holes is .apprx.15-25 .mu. thick. Second through-holes can be formed through the 1st and 2nd insulating layers, for the purposes of mounting electronic devices. Since the board has only 1 of the **elec. conductive circuit layers** exposed the other placed between 2 insulating layers of the laminate, the d. of wiring and of components can be much improved.

L40 ANSWER 57 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1976:570691 HCAPLUS
DN 85:170691
TI Substrates for printed circuits
IN Nomura, Hirotoshi
PA Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 51089581	A2	19760805	JP 1975-15767	19750205
	US 4029845	A	19770614	US 1975-603948	19750812
	DE 2536152	A1	19760226	DE 1975-2536152	19750813
	DE 2536152	C2	19821125		
	AU 7583954	A1	19770310	AU 1975-83954	19750814
	GB 1525012	A	19780920	GB 1975-33892	19750814
PRAI	JP 1974-93940		19740815		
	JP 1974-99765		19740829		
	JP 1975-15766		19750205		
	JP 1975-15767		19750205		

AB Metal foils or plastic films, which can be removed mech. or chem., are coated with a varnish contg. epoxy resin nitrile rubbers, and appropriate hardening agent, then films or foils are placed on **thermosetting resin** plates (prepregs) so that the varnish layers are contacted with prepregs, the composite plates are then hot-pressed until the prepregs and the varnish layers are simultaneously hardened, and the plastic films or metal foils are removed to give a laminate which is suitable as a substrate for a printed-circuit board on which **elec** . **conductive** materials are electroless and electroplated. The hot-pressing improves the hardness of the adhesive layer and hence reduces the undercut during the eteching of the elec. **conductor** layer. Thus, nitrile rubber 100 and epoxy resin (novolak-type) 100 wt. parts were kneaded, then Nadic Methyl Anhydride 100 wt. parts was added, and the mixt. was dissolved in MeCOEt to give a varnish. Thus, Al foils were coated with the varnish (15-20 .mu.), then the Al foils were placed on both sides of several sheets of phenolic resin prepregs, then composite material was hot-pressed at 160.degree. for 60 min, and the Al foils were mech. removed to give a laminated substrate. The substrate was electroless Ni plated, pattern coated with resist ink, then electroplated in Cu pyrophosphate bath, the resist ink and Ni layer were then removed to give a printed circuit having good soldering resistance and good adhesion of the **conductor** pattern with the substrate.

L40 ANSWER 59 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1971:534931 HCAPLUS
DN 75:134931
TI Microelectronic interconnection substrate
IN Leinkram, Charles Z.; Prom, Richard L.
PA United States Dept. of the Navy
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 3607379	A	19710921	US 1968-699724	19680122
PRAI US 1968-699724		19680122		

AB A single microelectronic interconnection substrate is fabricated for use in hybrid microelectronics capable of Au-Si eutectic bonding, thermal compression bonding, ultrasonic wire bonding, parallel gap welding, or Sn-Pb soldering. The substrate consists of an **insulating base** and 3 metal films, for example, a 1st Cr film, a 2nd Au film metallurgically bonded to the Cr film, and a 3rd Ni film bonded to the Au. The interconnection substrate is prepd. by sequential deposition of Cr, Au, and Ni onto a ceramic wafer. Alternatively, the Ni film may be plated by other conventional methods. The desired circuit is then etched photolithog. to produce Ni pads for Sn-Pb soldered or welded connections. A 2nd etching is done to produce Au pads suitable for thermal compression bonding, ultrasonic wire bonding, and Au-Si eutectic bonding. Circuit elements in the form of chips are then connected to the connection substrate and the entire unit is enca

L40 ANSWER 60 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1970:22684 HCAPLUS
DN 72:22684
TI Coating for the enhancement of solderability
IN Polereczky, Gabor; Radai, Sandor; Varga, Sandor; Varkonyi, Maria
PA Erdokemia Erdogazdasagi Vegyi es Ipari Vallalat
SO Hung., 8 pp.
CODEN: HUXXAT
DT Patent
LA Hungarian
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
HU 156458		19690922	HU	19661011

AB A coating is described for printed circuits, which, besides having advanta geous mech. and anticorrosive properties, facilitates soldering without removal of the coating. Thus, a soln. of pine resin 19 and Manila copal 1 in PhMe 40 and xylene 40 parts was homogenized in 1:1 ratio with a soln. of polyisobutylene (d.p. 1000) 2 and polyisobutylene (d.p. 5000) 6 in PhMe 46 and xylene 46 parts, the mixt. dild. with 8 parts iso-PrOH, and the whole stirred thoroughly 30 min.

L40 ANSWER 61 OF 62 HCAPLUS COPYRIGHT 2003 ACS
AN 1969:504648 HCAPLUS
DN 71:104648
TI Soldering inhibitor coat
IN Polareczky, Gabor; Varkonyi, Maria; Radai, Sandor; Varga, Sandor; Juhasz, Koppany
PA Beloiannisz Hiradastechnikai Gyar
SO Hung., 6 pp.
CODEN: HUXXAT
DT Patent
LA Hungarian
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
HU 156112		19690628	HU	19661202

AB A mixt. of cellulose ester and (or) ether 4-16, hydrogenated naphthalene deriv. or terpene alc. 27-70, additive (silica gel, surfactants) 0.5-15.0, and alkydamine resin 5-20% is applied to a printed-circuit plate, previously covered with colophony, with the exception of the points to be soldered, the cover is dried for 3 hrs. at 20.degree. or 20 min. at 60.degree.. Just before soldering, the whole plate is covered with a 30% soln. of colophony in iso-PrOH, then it is passed through a Flowsolder app. The solder moistened only those points which were not treated with the above mixt.

L41 ANSWER 14 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:551484 HCAPLUS
DN 133:170948
TI Fire-resistant circuit board substrates
IN Ohbayashi, Takashi; Omoya, Kazunori; Harada, Mitsuru; Kawakita, Yoshihiro
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000223809	A2	20000811	JP 1999-23400	19990201
	JP 3245400	B2	20020115		
PRAI	JP 1999-23400		19990201		

AB The title substrates are prepd. from a compressible porous polymer-impregnated fiber sheet which has **conductor**-plugged through holes to interconnect between metal **circuit films** formed on both sides of the substrate. The substrates are compressed to compact the plugged **conductor** for increased **elec. cond.** The impregnant polymer to the fiber sheets contains 3-30 wt.% N, P, and/or Si in its epoxy curing agent. The epoxy curing agent may be melamine-benzoguanamine-reformed Novolak polymer, melamine-reformed Novolak polymer, benzoguanamine-reformed epoxy resin, silicone-reformed epoxy resins, and/or cyclophosphazene-reformed polyamines. The substrates give increased fire resistance and decreased contact resistance.

L41 ANSWER 15 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:254749 HCAPLUS
DN 132:266264
TI **Electrically conductive** adhesives with high adhesion strength at room temperature and good reworkability
IN Matsuo, Yuki; Harada, Atsushi; Kimura, Koji
PA Murata Mfg. Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000113728	A2	20000421	JP 1998-282708	19981005
PRAI	JP 1998-282708		19981005		

AB The adhesives for mounting electronic parts on elec. **circuit substrates** comprise epoxy resins, **elec. conductive** powders, and polysulfones. Thus, an adhesive compn. contg. 100 vol.% mixt. of bisphenol A epoxy resin and 7% polysulfones and 5 vol.% conductive powders was applied between 2 pieces of Al2O3 test pieces and cured at 120.degree. for 30 min and then at 210.degree. for 20 min to give a cured product with adhesion strength 190 and 11 kg/cm2 at 25 and 220.degree., resp. and good reworkability.

L41 ANSWER 16 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:783531 HCAPLUS
DN 132:29575
TI IVH multilayer circuit boards and fabrication thereof
IN Ohira, Hiroshi; Saito, Toru; Matsuda, Norio; Urasaki, Yoshio
PA Yamaichi Electric Co., Ltd., Japan; Yamashita Circuitech K. K.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11340631	A2	19991210	JP 1998-144761	19980526
PRAI	JP 1998-144761		19980526		

AB The title inner via-hole (IVH) type circuit boards has an interlayer which is bound between **circuit layers**, has conductive connection between one **circuit layer** to its opposed **circuit layer** through connecting holes, and made from an anisotropic adhesive **conductor** to bind the opposed layers mech. and insulatively. At least portions of the opposed **circuit layers** are projected or recessed so that the press lamination gives the connection portions of the adhesive a prioritized pressure for providing an **elec. connection** with a tapered connection and the remainder portions left as an insulator.

L41 ANSWER 17 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:733820 HCAPLUS
DN 131:345298
TI Carboxyl-containing polyunsaturated fluxing adhesive for attaching integrated circuits
IN Zhou, Zhiming; Capote, Miguel A.
PA Capote; Miguel Albert, USA
SO U.S., 13 pp., Cont.-in-part of U.S. Ser. No. 897,968.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5985456	A	19991116	US 1997-926159	19970909
	US 5985043	A	19991116	US 1997-897968	19970721
	US 1998-137971	A2	19980821		

AB A thermally curable adhesive compn. including a fluxing agent that also acts as an adhesive is provided. The compn. includes: (a) a fluxing agent RCOOH, where R comprises a moiety having .gtoreq.2 C-C double bonds in which in 1 embodiment, .gtoreq.1 is within an acrylate or methacrylate group, and which may further contain .gtoreq.1 arom. moiety; (b) optionally, an effective amt. of a crosslinkable diluent; (c) optionally, an effective amt. of a source of free radical initiators; and (d) optionally, an effective amt. of a resin to react with remnant carboxylic acid moieties. By employing an acrylate, methacrylate, or phenol in the structure of the adhesive flux, the curing temp. and moisture absorption characteristics can be significantly improved. The compn. can be applied directly to the surface(s) of devices that are to be joined elec. and mech. These devices include printed **circuit substrates**, connectors, components, cables, and other elec. devices having metalization patterns to be soldered together by means of a solder-bumped pattern on 1 or both surfaces. Alternatively, a solder paste comprising solder powder mixed with the fluxing agent of the invention can be used. During the reflow step, the fluxing agent promotes wetting of the solder to the metalization patterns and, simultaneously, the fluxing agent itself crosslinks to mech. bond and encapsulate the surfaces and their metalizations. The compns. can also be used to formulate sinterable conductive inks.

L41 ANSWER 18 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:689061 HCAPLUS
DN 131:305958
TI Multilayer printed circuit boards having conductive paste-plugged via holes and fabrication thereof
IN Sato, Jiro; Matsuda, Hideki
PA Asahi Chemical Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11298105	A2	19991029	JP 1998-94973	19980407
PRAI	JP 1998-94973		19980407		

AB The title circuit boards comprise an insulative polymer substrate, an adhesive layer coated on the both sides of the substrate, a Cu circuit pattern laminated on the adhesive layer on the both sides of the substrate, and via holes provided through the adhesive/substrate/adhesive laminate and plugged with a conductive paste. The via hole plugs are covered by the Cu **circuit layers** on their ends. The substrate may be glass epoxy plate. The adhesive may be epoxy resin. The conductive paste comprises a conductive powder and a thermosetting polymer and is solidified in the via holes by heating.

L41 ANSWER 19 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:619127 HCAPLUS
DN 131:251419
TI Manufacture of multilayered printed circuit board
IN Sugimura, Takeshi; Negishi, Harumi; Mizuno, Yasuyuki; Fujimoto, Daisuke
PA Hitachi Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11266083	A2	19990928	JP 1998-66941	19980317
PRAI	JP 1998-66941		19980317		

AB Metal-clad **circuit substrates** prepd. by heat-pressing of prepregs are treated with acid before heat-press lamination with prepregs. The prepregs are manufd. by impregnation of reinforcement substrates with **thermosetting resin** compns. comprising cyanate esters, polyphenylene ether resins, monovalent phenols, flame retardants that are inactive against cyanate esters, and metallic reaction catalysts. The printed circuit boards have excellent solder heat resistance even after moisture adsorption.

L41 ANSWER 20 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:253879 HCAPLUS
DN 130:297621
TI Double-sided adhesive film for connecting electric circuits
IN Nagai, Akira; Watanabe, Itsuo; Takemura, Kenzo; Watanabe, Osamu; Isaka, Kazuhiro; Kojima, Kazuyoshi
PA Hitachi Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11106714	A2	19990420	JP 1997-276195	19971008
PRAI	JP 1997-276195		19971008		

AB The double-sided adhesive film is characterized by peeling forces of 2 surfaces, wherein the surface contacting a support is weaker than that of the other surface. The adhesive may be based on an epoxy resin, an acrylic rubber, and a latent hardening agent, and may contain dispersed **elec. conductive** inorg. particles with a diam. larger than that of an inorg. filler. This adhesive film is used for connecting IC chips and electronic components with a **circuit substrate**.

L41 ANSWER 21 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:139704 HCAPLUS
DN 130:176157
TI Printed circuit boards having through holes coated by conductive pastes
IN Shirai, Takahiro
PA Nippon CMK K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11054854	A2	19990226	JP 1997-225707	19970807
PRAI	JP 1997-225707		19970807		

AB The title circuit boards comprise a laminated insulative phenolic or epoxy resin substrate, a Cu-film **circuit layer** on the front and rear surface of the substrate, through holes provided to connect the front and the rear sides of the substrate, a through hole land provided around the through hole opening areas, a conductive paste filled in the through holes and coated around their opening area, and an overcoating material formed over the paste-coated opening areas. The powd. conductive material in the pastes may be Ag. The circuit boards have a dummy through hole which is empty and is provided between the paste-filled through holes so as to prevent migration of powd. circuit metal in the paste between potential-differentiated paste-coated through holes.

L41 ANSWER 22 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:136853 HCAPLUS
DN 130:171799
TI Method for aging **glass** bottles
IN Gallart Gabas, Jesus
PA Spain
SO PCT Int. Appl., 18 pp.
CODEN: PIXXD2
DT Patent
LA Spanish
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9908973	A1	19990225	WO 1998-ES231	19980814
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	ES 2136556	A1	19991116	ES 1997-1800	19970814
	ES 2136556	B1	20000901		
	ES 2149699	A2	20001101	ES 1998-1711	19980807
	ES 2149699	B1	20020201		
PRAI	ES 1997-1800	A	19970814		
	ES 1998-1711	A	19980807		

AB The process, for subjecting the bottles to a process of aging, coloration, and decoration, comprises a series of phases in closed circuit, from the supply of bottles to a conveyor to subject the bottles to various treatments, means for applying a wet coating to the bottles, heating means, means for chem. treating the surface of the bottles, means for painting the bottles, and means for curing the **thermosetting resin** applied to the bottles. The **thermosetting resin** contains opaque epoxy resin 50, clear epoxy resin 10, black epoxy resin 10, and talc 30 wt.%.

L41 ANSWER 23 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:512296 HCAPLUS
DN 129:210277
TI Manufacture of laminate circuit boards
IN Oto, Noriyasu; Naki, Akira
PA Matsushita Electric Works, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10215073	A2	19980811	JP 1997-18195	19970131
PRAI	JP 1997-18195		19970131		

AB The title process comprises laminating a no. of substrates for inner **circuit layers** and prepregs from a **thermosetting resin** compn. and a supporting material, fastening of the laminate with eyelet pins, placing a metal foil on both surfaces of the laminate with folding of the foil on the edges of the laminate, and supplying an elec. current to the foil for press resistance-heating of the laminate. The laminate prepd. has high precision of alignment and good forming.

L41 ANSWER 24 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:126200 HCAPLUS
DN 128:238022
TI Fabrication of printed circuit boards
IN Hagimura, Atsushi; Tanaka, Akisuke; Fujita, Kazuto; Shima, Kenji; Sakuraba, Hitoshi; Asahina, Kotaro
PA Mitsui Toatsu Chemicals, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10051136	A2	19980220	JP 1997-135520	19970526
PRAI	JP 1996-133984		19960528		
	JP 1996-135513		19960529		
	JP 1996-135514		19960529		

AB A 1st thermosetting polymer in bump contacts and a **circuit substrate** in the title fabrication employs a polymer having glass transition temp. at .gtoreq.250.degree. and Barcol hardness .gtoreq.45 at 200.degree.. A 2nd thermosetting polymer in a plastic substrate having contact holes employs a polymer having a viscosity 500-3000 Pa.s at 130.degree. and a viscosity increasing rate .ltoreq.5-times after 20 min at 130.degree.. The title fabrication involves press-laminating the 1st and 2nd polymer sheets by penetrating the bump contacts into the circuits on the 2nd substrates. The thermosetting polymers may be epoxy-/phenolic-polymer-modified polymaleimide polymers for properly laminating and connecting the bump contacts.

L41 ANSWER 25 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:42001 HCAPLUS
DN 128:102922
TI Electric conductive paste and manufacture of electric circuit board from the paste
IN Sasaki, Akihiro; Hirai, Keizo; Wada, Hiroshi; Yamana, Akizo
PA Hitachi Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10492310 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10007884	A2	19980113	JP 1996-128769	19960523
PRAI	JP 1995-124907		19950524		
	JP 1995-124908		19950524		
	JP 1996-100740		19960423		

AB The paste, having good **elec. cond.**, good storage stability and good Cu foil adhesion, comprises an **elec. conductive** powder, an alkoxy resolic phenolic resin made from an alkyl-substituted (bi)phenol, an aldehyde and an. alkyl alc., and a solvent, where the paste is used to bonding of Cu foil to an elec. **circuit substrate**. Thus, a paste was prepd. from a mixt. of Hitanol 4010 12, Cu flake 100, R 367 2, oxalic acid 0.3 and butyl Cellosolve 20 parts.

L41 ANSWER 26 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:614203 HCAPLUS
DN 127:271232
TI Multilayer printed circuit boards and fabrication thereof for prevention of crack formation
IN Katori, Naoya
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 15

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09232705	A2	19970905	JP 1996-36081	19960223
	JP 3301908	B2	20020715		
	JP 1996-38463	A	19960226		
	JP 1996-38464	A	19960226		

AB The insulative substrates for the title circuit boards comprise 60-95 wt.% powd. inorg. insulator and 5-40 wt.% thermosetting polymer. The circuit materials to be printed on the substrates comprise (1) powd. metals chosen from Sn-In, Sn-Bi, and Sn-Zn alloys and (2) a thermosetting polymer. The fabrication involves printing a circuit pattern with the circuit material on a green sheet of the insulative substrate and baking the green sheet together with the printed circuit pattern. The circuit boards are crack-free and chip-off-free against external force and thermal stress.

L41 ANSWER 27 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:369592 HCAPLUS
DN 126:344312
TI Lightweight prepreg containing resin-impregnated porous para-oriented aromatic polyamide film, its preparation and their use for printed **circuit substrate**
IN Takahashi, Tsutomu; Tsujimoto, Yoshifumi; Kumada, Hiroaki; Sato, Hiroyuki
PA Sumitomo Chemical Company Limited, Japan
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 768334	A2	19970416	EP 1996-116329	19961011
	EP 768334	A3	19970604		
	R: DE, FR, GB, IT, NL				
	JP 09324060	A2	19971216	JP 1996-256033	19960927
	TW 430678	B	20010421	TW 1996-85112496	19961014
	CA 2187857	AA	19970417	CA 1996-2187857	19961015
	US 5851646	A	19981222	US 1996-732577	19961015
PRAI	JP 1995-267040	A	19951016		
	JP 1996-78739	A	19960401		

AB Lightwt. prepreg having uniform thickness, low linear thermal expansion coeff. and good mech. strength, useful for printed **circuit substrate**/board, comprises a porous para-oriented arom. polyamide film (network or nonwoven fibril structure) impregnated with a thermoplastic resin and/or the **thermosetting resin**. Thus, a soln. contg. 2.0% poly(p-phenyleneterephthalamide) (PPTA, prepd. by polymn. of p-phenylenediamine and terephthaloyl dichloride) was cast on a **glass** plate and maintained 60.degree. for 20 min to form a white film, then was immersed in deionized water to elute the N-methyl-2-pyrrolidone solvent and calcium chloride to give a porous film which was sandwiched between filter paper and **glass** cloth, coated with a nylon film and sealed between nylon film and aluminum plate to form a prepreg with tensile strength in the application direction 9.0 kg/mm2, elongation 6.7% and linear thermal expansion coeff. -6.2 x 10-6/.degree..

L41 ANSWER 28 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:165104 HCAPLUS
DN 126:165104
TI Anisotropic **conductor** sheets laminated between conductive layers and electric circuit boards using thereof
IN Akagawa, Masatoshi
PA Shinko Elec Ind, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08330356	A2	19961213	JP 1996-7613	19960119
	US 5677576	A	19971014	US 1996-618807	19960320
	EP 734065	A2	19960925	EP 1996-301937	19960321
	EP 734065	A3	19970305		
	EP 734065	B1	20020619		
	R: DE, FR, GB				
	EP 786808	A1	19970730	EP 1997-300275	19970117
	EP 786808	B1	20020410		
	R: DE, FR, GB				
	US 6121688	A	20000919	US 1998-168148	19981008
PRAI	JP 1995-65609	A	19950324		
	JP 1996-7613	A	19960119		
	US 1997-786615	A1	19970117		

AB The title circuit boards have a pl. no. of patterned circuit/anisotropic-**conductor** laminated on a substrate and connectors connecting between adjacent circuits via interconnectors bump contacts through the anisotropic-**conductor** layers. The anisotropic-**conductor** layers are made of an **elec. conductive** metal flake filler dispersed in a polymer film. The interconnectors are formed to connect the **circuits layers** by pressing desired spots of the anisotropic conductive layers over bump contacts which are formed on the circuits in the desired connecting positions.

L41 ANSWER 29 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:165039 HCAPLUS
DN 126:165373
TI Electric capacitors built in circuits and fabrication thereof
IN Kikuchi, Junichi; Yamana, Shozo; Kuwajima, Hideji; Ono, Riichi; Ueda, Toyoichi
PA Hitachi Chemical Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08330181	A2	19961213	JP 1995-132364	19950530
PRAI	JP 1995-132364		19950530		

AB The title capacitors are prepd. by laminating conductive-paste/dielec.-paste double layer(s) between **conductor** layers formed on a **circuit substrate**. The conductive and dielec. pasts contain powd. metallic **conductor** and powd. dielec. material each mixed in polymer binders. The capacitors are thin-films and durable for bending.

L41 ANSWER 30 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:748140 HCAPLUS
DN 126:32693
TI Continuous fiber-free, electrically insulating double layer adhesive films and manufacture of multilayer printed circuits
IN Tanaka, Masashi; Ikeda, Kenichi; Tanaka, Katsuhiko; Suzuki, Takayuki
PA Hitachi Chemical Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08259912	A2	19961008	JP 1995-69043	19950328
PRAI	JP 1995-69043		19950328		

AB The title films comprise double layer **thermosetting resin** adhesives having different softening temp. (T), which are prepd. by coating adhesive varnish on base films, heating to cure to B stage, overcoating thermosetting adhesives, and heating to cure to B stage. The films are sandwiched with inner **circuit layers** and outer **circuit layers** (the lower-T layers are on the inner circuits) and heat-pressed to give multilayer circuit showing prevention of metal ion migration at hot moist condition. Thus, PET base films were coated by a varnish contg. bisphenol A epoxy resin and a polyisocyanate in AcNMe2, heated at 100-150.degree. for 20 min, overcoated by the vanish, and heated at 100-150.degree. for 20 min to give title double layer adhesive films (T 80.degree. and 45.degree.), then an inner circuit was sandwiched with the films as described above, further sandwiched by 2 Cu foils, and pressed at 80-170.degree. for 40 min to give a fiber-free 4-layer printed circuit board showing no void after etching on the Cu foils and good resistance to stray current corrosion.

L41 ANSWER 31 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:672216 HCAPLUS
DN 125:290939
TI Metal substrate for electric circuit
IN Kobayashi, Makoto; Nakajima, Yukio; Imamura, Kazuhiko; Okamoto, Kenji
PA Nippon Rika Kogyosho Kk, Japan; Fuji Electric Co Ltd
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08236884	A2	19960913	JP 1995-38498	19950227
PRAI JP 1995-38498		19950227		

AB The metal substrate comprises a heat-releasing metal base successively coated with (on .gtoreq.1 side) an insulating body (comprising 1st- and 2nd insulating layer) and conductive layer; wherein the 1st insulating layer is a **glass** fiber nonwoven fabric coated with an inorg. filler-contg. resin of compn. of Al oxide 48-75, B nitride 1-25, SiO2 1-10, and **thermosetting resin** 20-50 parts, and the 2nd insulating layer is a **thermosetting resin**-applied and -impregnated polyamide fiber nonwoven fabric (optionally contg. a **glass** fiber). A 3rd insulating layer composed of Si oxide 50-75, B nitride 1-25, SiO2 1-10, and a **thermosetting resin** 20-50 parts may be applied on the insulating body at the conductive layer side. The substrate shows excellent heat-releasing property, high voltage resistance, and heat resistance.

L41 ANSWER 32 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:910796 HCAPLUS
DN 123:356591
TI Copper powders and **electrically conductive** pastes
IN Mya, Yoshihiro; Kikuchi, Noburu; Oomaeda, Yuri
PA Hitachi Chemical Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07226110	A2	19950822	JP 1994-14297	19940208
PRAI	JP 1994-14297		19940208		

AB The Cu powders are surface-treated with C4-12 chain aliph. primary amine. The amine compd. in 0.1-1.0 parts to 100 parts Cu powder may be used. The **elec. conductive** pastes contain 10-40-part binder and 0.5-5-part dispersant to 100-part Cu powders. The binder may be a resol phenolic resin, an epoxy resin, or a photosensitive polyimide resin. The dispersant may be chain fatty acid alkali salt. The Cu powders in the elec. paste have oxidn. resistance and storage stability. The elec. paste is screen-printed on a **circuit substrate** and heated to give a hardened film having good **elec. cond.** and durability.

L41 ANSWER 33 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:795763 HCAPLUS
DN 123:215405
TI Anisotropic electrically conducting film
IN Myamoto, Tetsuya; Kawada, Masakazu
PA Sumitomo Bakelite Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07173448	A2	19950711	JP 1993-318704	19931217
PRAI	JP 1993-318704		19931217		

AB The film is obtained by applying a mixt. contg. (A) a poly(vinyl acetal), (B) an epoxy resin, (C) a microencapsulated imidazole deriv. of an epoxy compd., (D) a solvent, and (E) metal-coated spherical polymer conducting particles (particle size 3-15 .mu.m, av. size 5-10 .mu.m), on a releasing film and evapg. the solvent. The film shows good storage stability and is useful for **elec. connection** of liq.-crystal displays and flexible **circuit substrates**, etc.

L41 ANSWER 34 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:772867 HCAPLUS
DN 123:157940
TI Anisotropic, **electrically conductive** adhesive film and electronic assembly using it
IN Yamaguchi, Hiroaki
PA Minnesota Mining and Mfg. Co., USA
SO PCT Int. Appl., 19 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9516998	A1	19950622	WO 1994-US14468	19941216
	W: CN, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	JP 07211145	A2	19950811	JP 1993-316390	19931216
	EP 734576	A1	19961002	EP 1995-905956	19941216
	EP 734576	B1	20010404		
	R: DE, FR, GB				
	CN 1137324	A	19961204	CN 1994-194476	19941216
PRAI	JP 1993-316390	A	19931216		
	WO 1994-US14468	W	19941216		

AB The film comprises an insulating adhesive with **elec. conductive** particles and transparent, spherical glass particles dispersed in it. An electronic assembly, esp. an integrated circuit chip, is bonded to a **circuit substrate** by means of the adhesive film.

L41 ANSWER 35 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:638382 HCAPLUS
DN 123:72347
TI Connecting member of a **circuit substrate** and method of manufacturing multilayer **circuit substrates** by using the same
IN Nakatani, Seiichi; Hatakeyama, Akihito; Kawakita, Kouji; Sogou, Hiroshii; Ogawa, Tatsuo; Kojima, Tamao
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Eur. Pat. Appl., 23 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 645950	A1	19950329	EP 1994-114796	19940920
	EP 645950	B1	19980902		
	R: DE, FR, GB				
	JP 07147464	A2	19950606	JP 1994-211074	19940905
	JP 2587596	B2	19970305		
	CN 1108026	A	19950906	CN 1994-113752	19940920
	CN 1075338	B	20011121		
	US 5484647	A	19960116	US 1994-308982	19940920
	US 6108903	A	20000829	US 1996-582930	19960104
	US 2001003610	A1	20010614	US 2001-769260	20010126
PRAI	JP 1993-234519	A	19930921		
	JP 1993-242450	A	19930929		
	US 1994-308982	A3	19940920		
	US 1996-582930	A1	19960104		
	US 1999-259966	A1	19990301		

AB A connecting member of **circuit substrates** includes an org. porous base material provided with tackfree films on both sides, through holes disposed at desired places which are filled with conductive resin compd. up to the surface of the tackfree films. This structure enables inner-via-hole connection and can therefore attain a connecting member of **circuit substrates** and an **elec. connector** of high reliability and high quality.

L41 ANSWER 36 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:619335 HCAPLUS
DN 121:219335
TI Anisotropic **electrically conductive** adhesives
IN Funahashi, Hajime; Koizumi, Masakazu
PA Fuji Polymer Ind, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06052715	A2	19940225	JP 1992-203793	19920730
PRAI	JP 1992-203793		19920730		

AB Title adhesive paste or film for **elec. connecting** by hot-pressing to **circuit substrates** comprises 65-95 wt.% epoxy-modified thermosetting polymer as an adhesive matrix, a hardening agent, metal or metal-coated particles as an **elec. conductive** material, and an epoxylated alkoxysilane coupling material, wherein the hardening agent is encapsulated. The encapsulated hardening agent gives the adhesives an increased stable storage period and an increased reactivity for adhesion.

L41 ANSWER 37 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:93381 HCAPLUS
DN 120:93381
TI Ceramic **circuit substrate**
IN Ootani, Hiroyuki
PA Matsushita Electric Ind Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05206598	A2	19930813	JP 1992-12755	19920128
PRAI	JP 1992-12755		19920128		

AB The title substrate is formed by laminating a conductive polymer film and a metal film successively on a multilayer ceramic substrate. The arrangement gives the substrate an increased adhesion of the metal film on the multilayer ceramic substrate to eliminate a thermal stress.

L41 ANSWER 38 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:639823 HCAPLUS
DN 119:239823
TI Ceramic-polymer composite circuit board
IN Demura, Akihiro
PA Ibiden Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05082929	A2	19930402	JP 1991-273187	19910924
PRAI	JP 1991-273187		19910924		

AB The title circuit board comprises a ceramic substrate/ **thermosetting resin** composite insulator layer and a metal layer laminated on the composite insulator layer, wherein the size of the ceramic substrate is smaller at its periphery and substituted at its recessed edge area with the resin material, i.e., only resin layers are appears at its cross section of the laminate side edges. The arrangement of the ceramic and resin sizes prevents heat-generated cracks and peeling of the laminates.

L41 ANSWER 39 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:571640 HCAPLUS
DN 119:171640
TI Void-suppressed multilayer printed circuit board
IN Ito, Shigeru; Mitsuhashi, Kazunori
PA Shin-Kobe Electric Machinery Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04372194	A2	19921225	JP 1991-149101	19910621
	JP 2917579	B2	19990712		
PRAI	JP 1991-149101		19910621		

AB The title circuit board comprises: an outer circuit insulator layer of a **thermosetting resin**-impregnated **glass** woven fabric and an inner circuit insulator layer bonded to the outer **circuit layer** through an adhesion layer of a **thermosetting resin**-impregnated **glass** fiber-arom. polyamide nonwoven blend.

L41 ANSWER 40 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:561946 HCAPLUS
DN 119:161946
TI Fluorescent laminates, printed **circuit substrates**, and circuit inspection
IN Yamagami, Mamoru; Tsujioka, Norio
PA Asahi-Schwebel Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05009309	A2	19930119	JP 1991-160541	19910701
PRAI	JP 1991-160541		19910701		

AB The laminates are manufd. by hot-pressing **glass** cloth-reinforced **thermosetting resin** prepregs contg. silane coupling agents with 490-700-nm fluorescence excitable at .apprx.442 nm. The boards are manufd. by laminating the fluorescent laminates obtained, on one or both sides, with metal foil. The inspection can be performed by exposing the multilayer-plate surfaces to light with certain wavelengths to excite the fluorescence and then comparing the fluorescent emission pattern with that of the intended circuit.

L41 ANSWER 41 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:582950 HCAPLUS
DN 117:182950
TI Copper laminate for multilayer printed-circuit board
IN Nakamura, Toshio; Amano, Masayuki
PA Hitachi Kasei Kogyo K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04094187	A2	19920326	JP 1990-211240	19900809
PRAI	JP 1990-211240		19900809		

AB The title Cu laminate is made up of a **glass** fiber substrate impregnated with a **thermosetting resin**, an inner **circuit layer** on 1 or both sides of the substrate, and a Cu foil adhered to the inner **circuit layer** by a **thermosetting resin**. This Cu laminate gives excellent stability against thermal shock.

L41 ANSWER 42 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:596337 HCAPLUS
DN 115:196337
TI Printed circuit multilayer boards
IN Ito, Shigeru; Mitsuhashi, Kazunori; Sakaguchi, Tatsu; Suirenya, Ichiro; Kimura, Hiromitsu
PA Shin-Kobe Electric Machinery Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03116894	A2	19910517	JP 1989-254527	19890929
	JP 07034506	B4	19950412		
PRAI	JP 1989-254527		19890929		

AB The title board is a thermally press-formed composite body comprising (1) internal **circuit substrates** by chem. surface-microroughened and **thermosetting resin** -impregnated nonwoven **glass** fiber, (2) outer surface circuit insulator layers by **thermosetting resin**-impregnated woven **glass** fiber, and (3) internal insulator layers by **thermosetting resin**-impregnated nonwoven **glass** fiber, wherein the resin for the internal **circuit substrates** contain 30-50 wt.% inorg. filler and for the internal insulator layers, 5-20 wt.% inorg. filler. The materials give an excellent cohesion to the lamination of the internal **circuit layers** and the internal insulator layers.

L41 ANSWER 43 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:525157 HCAPLUS
DN 115:125157
TI Manufacture of laminated boards for printed circuits
IN Konagaya, Hiroshi
PA Sumitomo Bakelite Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02258337	A2	19901019	JP 1989-78357	19890331
	JP 2894496	B2	19990524		
PRAI	JP 1989-78357		19890331		

AB The title board comprises surface layers made from a **glass** fiber impregnated with a **thermosetting resin** and interlayers made from a nonwoven **glass** fiber impregnated with a (10-200): 100 (wt. ratio) filler-**thermosetting resin** composite, wherein a metal film to be laminated on the surface and to form a printed circuit is a Cu film with its elongation percentage 5.5% per 10 .mu.m at 180.degree. and is baked after its lamination. The baking after the Cu film lamination gives the laminate an improved dimensional precision.

L41 ANSWER 44 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1988:446903 HCAPLUS
DN 109:46903
TI Adhesives for electroless coating of **circuit substrates**
IN Yamase, Yukio; Jida, Hiroyuki; Akazawa, Masashi; Miyasaka, Haruyuki
PA Nippon Soda Co., Ltd., Japan; Seiko Epson Corp.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 62248291	A2	19871029	JP 1986-92908	19860422
PRAI	JP 1986-92908		19860422		

AB The title **circuit substrates** have cured coatings of adhesives contg. synthetic rubber, a **thermosetting resin**, and imidazole-contg. compds. **Circuit substrates** showing almost no migration and moisture resistance are prepd. BKR 2620 (alkyl-modified phenol), Nipol 1042 (acrylonitrile-butadiene rubber), and Epikote 1001 (bisphenol-A-type epoxy resin) were dissolved in a solvent, mixed with Crystalite CMC-12 (fused silica) and 2-ethyl-4-methylimidazole to give an adhesive, which was applied on a Cu-clad **glass**-epoxy resin laminate and heat-cured to give a **circuit substrate**. No migration was obsd. in an circuit prepd. by electroless coating of the substrate by Cu.

L41 ANSWER 45 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1988:122988 HCAPLUS
DN 108:122988
TI Preparation of **circuit substrates** with hollow bead-containing core sheets
IN Okada, Reisuke; Yamamoto, Keiichiro
PA Toray Industries, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 62154690	A2	19870709	JP 1985-294464	19851226

PRAI JP 1985-294464 19851226

AB Prepn. of a **circuit substrate** by hot-press lamination of flat plates from a heat-cured thermosetting plastic, 1 of which contains small hollow bodies, involves hardening the plastic having small hollow bodies, and laminating another plate in the B stage with a Cu foil by hot-pressing. Epikote 828, Epiclon B 650, and Me2NBz were mixed with **Glass** Bubble B38/400 (hollow bodies) and cured and formed into a C-stage core sheet. B-stage prepregs, prepd. by impregnation of **glass** cloth with Epikote 1045, Epikote 145, dicyandiamide, and Me Cellosolve, and Cu foils were laminated on both sides of the prepd. core sheet and heat-pressed to give 1.6-mm substrate. No peeling or blistering was obsd. upon immersion in 260.degree. solder.

L41 ANSWER 46 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1988:113869 HCAPLUS
DN 108:113869
TI Printed **circuit substrate**
IN Maeda, Masahiko; Takaishi, Minoru; Yoshimura, Kazuhito
PA Showa Denko K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 62262487	A2	19871114	JP 1986-104854	19860509
PRAI JP 1986-104854		19860509		

AB The title substrate, having good heat resistance and dielec. properties, is prepd. by laminating a **thermosetting resin**-contg. layer and a metal foil with an adhesive comprising a copolymer of ethene and a copolymerizable C6-30 epoxy compd. and a copolymer of ethene and a monomer which reacts with epoxy groups at 300.degree. during 20 min to form ester linkages. An epoxy resin-impregnated **glass** cloth and a 17-.mu. Cu foil were laminated with a mixt. of 50 parts 20:80 acrylic acid-ethene copolymer and 50 parts 68.7:12.7:18.6 ethene-glycidyl methacrylate-Me methacrylate copolymer to give a substrate having good solder resistance, interlayer adhesion, and dielec. properties.

L41 ANSWER 47 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1987:525478 HCAPLUS
DN 107:125478
TI Electronic circuit boards
IN Saito, Shinji; Yamauchi, Hidetoshi
PA Ibiden Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 62126694	A2	19870608	JP 1985-266657	19851127
	JP 06034435	B4	19940502		
PRAI	JP 1985-266657		19851127		

AB The title product consists of a composite from a porous sintered ceramic (e.g., porosity <10 vol.%) of 3-dimensional framework having open pores (e.g., 10-70 vol.%) filled with resin, .gtoreq.1 resin layer (e.g., inorg fiber cloth layer impregnated with resin or inorg. fiber-resin composite) on the surface of the composite, and elec. circuit(s) on or between the resin layers, or on the composite surface. The ceramic may mainly comprise .gtoreq.1 of Al2O3, SiO2, ZnO, ZrO2, MgO, PbO, B2O3, Si3N4, BN, and AlN. The resin in the open pores may be an epoxy, polyimide, polyparabanic acid, polyamide imide, silicone, epoxy silicone, acrylic acid, methacrylic acid, phenolic, urethane, furan, fluorocarbon, triazine, or aniline resin. A circuit board consisting of epoxy-resin impregnated sintered sillimanite, a patterned Cu foil **circuit layer**, and an epoxy-resin impregnated **glass** cloth layer had no breakage in >2000 drillings.

L41 ANSWER 48 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:582274 HCAPLUS
DN 105:182274
TI Flexible **circuit substrate** with **electrically conductive** adhesive layer
IN Suzuki, Tameyuki; Kamakura, Takuro
PA Shinto Paint Co., Ltd., Japan
SO Ger. Offen., 18 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 3543924	A1	19860717	DE 1985-3543924	19851212
	US 4844784	A	19890704	US 1985-808140	19851212
PRAI	JP 1984-270302		19841220		

AB A flexible **circuit substrate** and a method for its fabrication are described in which the **elec. conductive** paths on the substrate are coated with an **elec. conductive** adhesive layer applied by electrodeposition of high-mol. wt. resins. The conductive paths may have widths of .ltoreq.0.1 mm and the sepn. between adjacent paths may be .ltoreq.0.2 mm. The conductive adhesive layer may contain fine particles of Ti carbide or Ti nitride. Applications to liq.-crystal, electrochromic, and electroluminescent devices are indicated.

L41 ANSWER 49 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:578392 HCAPLUS
DN 93:178392
TI Improved methods and apparatus for making copper substrates for printed circuits
IN Coillard, Christian
PA Constructions Mecaniques Electriques et Electroniques de Limours, Fr.
SO Eur. Pat. Appl., 10 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 12094	A1	19800611	EP 1979-400969	19791205
	EP 12094	B1	19820317		
	R: BE, DE, GB, IT, NL, SE				
	FR 2443787	A1	19800704	FR 1978-34248	19781205
	FR 2443787	B1	19820618		
PRAI	FR 1978-34248		19781205		

AB On a continuously moving ribbon of Cu, .gtoreq.1 ribbon of fiberglass and .gtoreq.1 layer of **thermosetting resin** are deposited. At least 50 wt.% of resin in the total is preferred. A 2nd ribbon of Cu or a ribbon of synthetic material may be superimposed. The assembly is then passed through an oven under pressure to cure the resin.

L41 ANSWER 50 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1977:99921 HCAPLUS
DN 86:99921
TI Prepreg sheets for printed **circuit substrates**
IN Shoji, Rikuo; Kitamura, Tsuneo; Arai, Minio; Mori, Yasuomi
PA Nihon Bairin Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 51138766	A2	19761130	JP 1975-62469	19750527
PRAI JP 1975-62469		19750527		

AB A **thermosetting resin**, hardening agent, and filler (.ltoreq.60 wt. % of the mixt.) are melt-kneaded, cooled, crushed, then the powder (120-400 wt. % with respect to the substrate) is placed evenly on a nonwoven fiber sheet (thickness 20-120 g/m2, bulk d. 0.15-0.50 g/cm3), and the sheet is heated so that the resin compn. in B-stage impregnates the sheet to give a prepreg sheet which is useful as an elec. insulating substrate for printed circuits. The method gives a prepreg contg. a uniformly distributed resin compn. (including the filler) in B-stage, and the prepreg sheets exhibit good size stability, good water resistance, and good elec. insulating properties. Thus, epoxy resin (Epikote 828 from Shell Chem. Co.) 20, another epoxy resin (Epikote 1001) 80, diaminodiphenylsulfone 12, and SiO2 powder 50 wt. parts were melt-kneaded, cooled, and crushed (-100 mesh) to give a resin compn. powder. The powder 300 at. % (with respect to the wt. % of a **glass** fiber sheet) was coated on an unwoven **glass** fiber sheet (thickness 0.3 mm, 60 g/m2, d. = 0.20 g/cm3) prepd. by using 9-.mu.-diam. 13-cm-long **glass** fiber and amine epoxide acidic salt type adhesive, then the sheet was heated at 170.degree. for 20 s by using an IR heater to give a prepreg. Eight prepreg sheets were then laminated with a 35-.mu.-thick Cu foil by hot-pressing at 165.degree., pressed for 30 min at 120 kg/cm2, and cured for 1 h to give a 1.74-mm-thick Cu laminate which satisfied all of the NEMA G-10 requirements.

L41 ANSWER 51 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1976:183860 HCAPLUS
DN 84:183860
TI Sensitized substrates for chemical metallization
IN Polichette, Joseph; Leech, Edward J.; Nuzzi, Francis J.
PA Kollmorgen Corp., Photocircuits Division, USA
SO U.S., 11 pp. Division of U.S. 3,772,056.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3925578	A	19751209	US 1973-387586	19730813
	US 3772056	A	19731113	US 1971-167432	19710729
	AT 321668	B	19750410	AT 1972-6389	19720725
	AT 7404112	A	19750415	AT 1972-411274	19720725

AB A process is disclosed for sensitizing and activating for electroless and electroplating nonconducting substrates such as thermoplastic and **thermosetting resins**, **glass**, ceramics, cloth, wood, and paper, by forming on them a nonconducting layer of metallic nuclei of Fe, Ni, Co, or preferably Cu, from a dried coating of an aq. soln. of metal salt. The solns. forming these nuclei can be used instead of the conventional SnCl2 and PdCl2 solns. for such sensitizing and activation. The 1st step of the present process is thorough cleaning of the substrate surface, which can include abrasive roughening, etching with CrO3 and H2SO4, or polarizing with DMF or Me2SO. The next step is dipping in the metal salt soln. for a few min, the metal being preferably Cu, and suitable salts being formate, gluconate, or acetate, with optional surfactants. This wet coating is dried at .ltoreq.170.degree., and can be exposed to radiant energy of various kinds, or chem. redn. by NaBH4, NaHCO3, aldehydes, or xanthenes, to form the darker-colored catalytic nuclei required for activation to receive adherent metal ions from any conventional chem.-plating soln. for the desired conductive deposit of Cu, Ni, Ag, Au, Rh, Sn, or Zn, esp. for printed circuits.

L41 ANSWER 52 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1975:25110 HCAPLUS
DN 82:25110
TI Stampable and boreable, fire-resistant insulator plate for electrical purposes
IN Nishi, Hiromichi; Furugoori, Akio; Hasegawa, Kinichi
PA Sumitomo Bakelite Co., Ltd.; Sansui Electric Co., Ltd.
SO Ger. Offen., 28 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2413158	A1	19741003	DE 1974-2413158	19740319
	DE 2413158	B2	19750821		
	DE 2413158	C3	19760325		
	JP 49120916	A2	19741119	JP 1973-33093	19730324
	JP 57036148	B4	19820802		
	JP 49120917	A2	19741119	JP 1973-33094	19730324
	JP 57036149	B4	19820802		
	GB 1468065	A	19770323	GB 1974-11488	19740314
PRAI	JP 1973-33093		19730324		
	JP 1973-33094		19730324		

AB Insulating substrates which could be bored or stamped were manufd. by bonding a thin **thermosetting resin** impregnated layer (e.g. epoxy impregnated **glass** cloth) to a thicker supporting plate. This plate contained 10-70 wt. % inorg. fibers (e.g. asbestos), 1-40 wt. % inorg. binder (e.g. cement), and the balance inorg. filler; the hardened plate was impregnated with a **thermosetting resin** amounting to .apprx.5 wt. %.

L41 ANSWER 53 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1974:28115 HCAPLUS
DN 80:28115
TI Insulating substrates for printed circuits
IN Shaul, Anthony J.; Wood, Edward Russell
PA Formica International Ltd.
SO Fr. Demande, 14 pp. Addn. to Fr. 2,080,597 (See S. African 71 01,017, CA 76;155020z).
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2158256	A2	19730615	FR 1972-37639	19721024
	GB 1395887	A	19750529	GB 1971-49443	19721017
	ZA 7207423	A	19740529	ZA 1972-7423	19721018
	AU 7247998	A1	19740426	AU 1972-47998	19721020
PRAI	GB 1971-49443		19711025		

AB Silicone sheets or parchment-like webs, silicone-treated Al plates, and polymer insulator substrates were treated with mixts. of polybutadiene [9003-17-2] or ABS latex, nitrile rubber or SBR and **thermosetting resins**, e.g. epoxy or phenol-formaldehyde resins [9003-35-4] and heat cured under pressure to give selectively attackable hard surfaces for printed circuit manuf. A laminated duraluminum plaque was coated with a phenylmethylsilicone resin; heat cured; topped with a mixt. of solvent, phenolic resin, hardener, and acrylonitrile-butadiene rubber; heated to remove solvent; cut into sheets which were assembled with 3 layers of **glass** fiber cloth preimpregnated with epoxy resin so that the rubberized surfaces contacted the epoxy resin, and the whole cured 35 min at 160-5.deg./49kg/cm2. The product was unmolded and the silicone-coated Al sheet removed leaving the cured, smooth surfaced rubber-resin composite, of good phys. quality for printed circuit manuf.

L41 ANSWER 54 OF 54 HCAPLUS COPYRIGHT 2003 ACS
AN 1974:16159 HCAPLUS
DN 80:16159
TI Flexible printed circuits from rubber-impregnated cloth
IN Watanabe, Tsutomu; Nakayama, Takahiro; Yamaoka, Shigenori
PA Sumitomo Bakelite Co., Ltd.
SO Jpn. Tokkyo Koho, 3 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 47042753	B4	19721028	JP 1968-87609	19681202

AB **Glass** or synthetic fiber fabric or paper was coated or impregnated with an elastomer-vulcanizing agent mixt., coated with a **thermosetting resin** to a wt. of 30-1700 g/m2, and laminated with a metal foil to give flexible printed **circuit substrates**. Thus, a mixt. of 80 parts nitrile rubber and 20 parts phenolic resol was coated on a silane-treated **glass** cloth to 25% resin content, an epoxy resin-m-tolylenediamine mixt. was coated on the cloth to an addnl. 21% resin takeup, and the impregnated material(360 g/m2) was pressed with a 35.mu. copper [7440-50-8] foil 50 min at 150.deg./30 kg/cm2 to give a laminate with superior flexibility, heat resistance in soldering, and mech. strength.

L59 ANSWER 17 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:161563 HCAPLUS
DN 132:215595
TI Conductive paste, conductive structure using the same, electronic part, module, circuit board, method for **electrical connection** , method for manufacturing circuit board, and method for manufacturing ceramic electronic part
IN Igaki, Emiko; Tanahashi, Masakazu; **Suzuki, Takeshi**
PA Matsushita Electric Industrial Co., Ltd., Japan
SO PCT Int. Appl., 60 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000013190	A1	20000309	WO 1999-JP4595	19990826
	W: CN, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 1050888	A1	20001108	EP 1999-940485	19990826
	R: DE, FR, GB				
	JP 2000215729	A2	20000804	JP 1999-242254	19990827
	US 6479763	B1	20021112	US 2000-530466	20000428
PRAI	JP 1998-244151	A	19980828		
	JP 1998-324699	A	19981116		
	WO 1999-JP4595	W	19990826		

AB A conductive paste used for mounting an electronic part on a board or connecting electrodes, a conductive structure using the paste, an electronic part, a module, a circuit board, a method for **elec. connection**, a method for manufg. a circuit board, and a method for manufg. a ceramic electronic part (all will be referred to as conductive paste and so forth) are disclosed. **Elec. connection** using conductive paste was used in various fields for its ease. The cond. of conductive paste is ensured by the contact between conductive particles in the conductive paste. Conventionally, stress is generated in conductive paste when it is heated, and the contact between conductive particles is partially broken when the stress is relaxed, causing a problem of high resistance. The conductive paste of the invention was characterized in that it contains conductive particles, a foaming material foamable when heated or depressurized, and a **resin** and it does not lose its cond. even after the foaming material is foamed. The base has a good stress resistance and enables low-resistance **elec. connection**.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 18 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:823987 HCAPLUS
TI **Circuit substrate** and its production method. [Machine Translation].
IN [NAME NOT TRANSLATED], Satoru; **Suzuki, Takeshi**; Ogawa, Tachio
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 2000323842	A2	20001124	JP 1999-133888	19990514
PRAI	JP 1999-133888		19990514		

AB [Machine Translation of Descriptors]. Offers with the method of producing the circuit baseplate and this circuit baseplate which make the constitution whose is possible to guarantee high connected reliability. It designates that as for the circuit baseplate 1 which relates to this invention and 11, suffering through the conductive powder 4 where the wiring pattern 3 companion which wears fills up inside penetration hole 6 on the surface of baseplate material 2, being something which continues is connected, as for the conductive powder 4 which fills up inside penetration hole 6, the mutual companion of conductive powder 4 is deposited, at the same time, also wiring pattern 3 being made to deposit, is as feature. In addition, when while baseplate material compressing 2 and metal foil 7 alongside thickness direction, heats the production method of the circuit baseplate 1 which, relates to this invention, at the same time, the electric conduction are done process, or the baseplate material 2 which and metal foil 7 while compressing alongside thickness direction heats the high piezoelectricities style between the wiring pattern 3 companion which was formed from metal foil 7 simultaneously, between the metal foil 7 companion the electric conduction after doing the high piezoelectricities style, includes the process which wiring pattern 3 the formation is done from metal foil 7.

L59 ANSWER 19 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:143990 HCAPLUS
TI **Circuit substrate** and its production method. [Machine Translation].
IN Nakatani, Yasuhiro; **Suzuki, Takeshi**
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000068620	A2	20000303	JP 1998-238580	19980825
PRAI JP 1998-238580		19980825		

AB [Machine Translation of Descriptors]. The inner buyer hole (IVH) improvement of connected reliability of the circuit baseplate which is connected and fine patterning of the wiring pattern are assured. Converts roughly the conductive compn. 2 which fills up to the penetration hole of insulator layer 1, surface of conductive compn. 3 of the wiring pattern 3 which is connected elec. in comparison with the surface of insulator layer 1.

L59 ANSWER 20 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:363963 HCAPLUS
DN 135:115398
TI Next generation ALIVH substrate for bare chip direct mounting
AU Andoh, Daizo; Sugawa, Toshio; **Nakamura, Tadashi**; Higashitani, Hideki; Eda, Kazuo; Tsukamoto, Masahide
CS Device Engineering Development Center, Matsushita Electric Industrial Co.,Ltd., Osaka, 571-8501, Japan
SO Proceedings - International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces, Braselton, GA, United States, Mar. 6-8, 2000 (2000), 227-232 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 69BHZK
DT Conference

LA English
AB The next generation ALIVH substrate named ALIVH-FB substrate was developed. The ALIVH-FB substrate has a structure that fine layers were formed on the surface of the conventional ALIVH substrate. The design rule of the core layer is Line/Space (L/S)=50/50 .mu.m, Via hole diam./Land diam. (V/L)=120/250 .mu.m and the rule of fine layer is L/S = 25/25 .mu.m, V/L = 50/150 .mu.m. Three technologies were developed (1) Thin insulator layer by the film material with high heat resistance, (2) fine via hole drilling process by the YAG THG laser and the fine interconnection technol. using the conductive Cu paste, (3) Fabrication process of the fine layers by the transfer process. The feature is following 4 points. (1) High wiring d. by the Fine Via on Via structure, (2) Film insulator with the high heat resistance and low CTE for the high reliability of the joint between the bare chip and the substrate, (3) Good impedance control for the high frequency circuit, (4) Flat surface and High heat resistance for the bare chip mounting. The ALIVH-FB substrate is very suitable for the high pin count bare chip direct mounting.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L59 ANSWER 21 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:814823 HCAPLUS
DN 132:57842
TI Printed circuit boards and fabrication thereof for increased adhesion
IN **Kawakita, Yoshihiro**
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11354899	A2	19991224	JP 1998-162096	19980610
PRAI	JP 1998-162096		19980610		

AB The interlayer insulator prepreg film bound between metallic **circuit films** is a glass or org. fiber which is impregnated with an insulative polymer. A P compd. such as phosphoric or phosphorus ester is deposited on the fiber surface for impregnation of the adhesive polymer and/or on the circuit-insulator interface. The deposition of the P compd. gives the conductor/insulator interface improvement of breakdown prevention and multilayer circuits increase of adhesion.

L59 ANSWER 22 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:56930 HCAPLUS
DN 130:132898
TI Prepreg for circuit board and manufacture of the prepreg and double-sided circuit board using it
IN Nakaya, Yasuhiro; Hatanaka, Hideo; Noda, Osamu; **Kawakita, Yoshihiro**; Ishimaru, Yukihiro; Hasegawa, Masao; Oohata, Tsumoru; Sakamoto, Kazunori
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11017295	A2	19990122	JP 1997-171422	19970627

PRAI JP 1997-171422 19970627

AB The manuf. of the prepreg involves the following steps: (1) applying an elec. insulating **resin** on .gtoreq.1 of two mold-release cover films at the mold-release side, (2) sandwiching thermosetting **resin**-impregnated fibrous sheet substrate, preferably glass-epoxy composite, glass-BT **resin** composite, aramid-epoxy composite, and/or aramid-BT **resin** composite between the release films and pressing the laminate, and (3) cutting the laminate into pieces. The prepreg obtained by the above method has an elec. insulating layer composed of a polyimide-siloxane, an aramid elastomer, and/or an indene oligomer and optionally **thermosetting epoxy resin** compns. and inorg. fillers between the sheet substrate and .gtoreq.1 mold-release cover film. The circuit board is manufd. by opening through holes on the above prepreg, filling the holes with an **elec. conductive** polymer compn. to the same level of the cover films, peeling the cover films from the prepregs to project the **elec. conductive** fillings, laminating metal foils or other circuit boards at the both sides of the prepreg, hot-pressing the laminate to cure the prepreg, and processing the metal foils to form circuit patterns on the both surface. In the method, another circuit board may be successively sandwiched between two prepregs and two pieces of metal foil, followed by hot-pressing the laminate and processing the foils to form multilayer circuit patterns. The insulating layer shows good adhesion to the prepreg layer to improve moisture resistance.

L59 ANSWER 23 OF 27 HCAPLUS COPYRIGHT 2003 ACS

AN 1999:722827 HCAPLUS

DN 131:331177

TI Conductive paste for filling via holes, double-sided and multilayer printed circuit boards using the paste, and production of the circuit boards

IN Omoya, Kazunori; **Suzuki, Takeshi**; Ogawa, Tatsuo; Oobayashi, Takashi

PA Matsushita Electric Industrial Co., Ltd., Japan

SO Eur. Pat. Appl., 36 pp.
CODEN: EPXXDW

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 955795	A2	19991110	EP 1999-108590	19990507
	EP 955795	A3	20010314		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000030533	A2	20000128	JP 1999-124454	19990430
	JP 3038210	B2	20000508		
	US 6139777	A	20001031	US 1999-304700	19990504
	CN 1236798	A	19991201	CN 1999-106371	19990510
PRAI	JP 1998-126412	A	19980508		

AB A paste for via-hole filling comprises at least (a) 30-70 vol.% conductive particles whose av. diam. is 0.5-20 .mu.m and whose sp. surface area is 0.05-1.5 m2/g, and (b) 70-30 vol.% **resin** comprising .gtoreq.10% **epoxy resin** comprising .gtoreq.1 epoxy group per mol., in which the total amt. of hydroxyl, amino, and carboxyl groups is .ltoreq.5 mol% of the epoxy groups, and the epoxy equiv. is 100-350 g/equiv. The conductive paste for filling via holes and a printed circuit board contg. them can be used to provide an inner-via-hole connection between electrode layers without using a through-hole plating technique.

L59 ANSWER 24 OF 27 HCAPLUS COPYRIGHT 2003 ACS

AN 1998:479330 HCAPLUS
DN 129:183017
TI Printing substrate having multilayer structure for the manufacture of printed circuit boards
IN **Suzuki, Takeshi**; Ishimaru, Yukihiro; Sakamoto, Kazunori; Ueda, Yoji
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10190159	A2	19980721	JP 1996-343966	19961224
PRAI JP 1996-343966		19961224		

AB The outermost layer in the printing substrate plays the role of a mask film, and the outer surface of the mask film is peelable. The mask film preferably consists of a synthetic **resin** (PETF or polypropylene) film and a parting agent coated thereon. **Elec. connectors** are obtained by forming through holes in the prescribed positions in the printing substrate and filling them with an **elec. conductive** compn. contg. 80-92 wt.% metal powder having an av. particle diam. 0.5-20 .mu.m and 4.5-10 wt.% **epoxy resin**, phenolic **resin**, polyimide **resin**, or acrylic **resin**. The printing substrate is utilized for the manuf. of multilayer printed circuit boards.

L59 ANSWER 25 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:135650 HCAPLUS
DN 128:237285
TI Liquid crystal display test device for testing electric connection of terminals
IN Ueki, Mitsuyoshi; Kato, Naoki; Matsuda, Atsushi; Ishii, Toshinori; Yoshida, Hideaki; **Nakamura, Tadashi**
PA Mitsubishi Materials Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10054845	A2	19980224	JP 1996-211283	19960809
JP 3132394	B2	20010205		
PRAI JP 1996-211283		19960809		

AB The test device comprises (1) a conduct probe contg. parallelly arranged contact pins vertically laminated on 1 side of a 1st non-**elec. conductive resin** film with the pin terminal parts out of the **resin** film, (2) a strong flexible film made of an org. or inorg. material on the above **resin** film with the terminal parts out of the **resin** film but shorter than the contact pins, (3) a contact probe holder, and (4) a frame for supporting the contact probe holder.

L59 ANSWER 26 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:802202 HCAPLUS
DN 128:135324
TI **Electrically conductive** filler composition containing solvent with restricted solubility parameter
IN **Suzuki, Takeshi**; Sakamoto, Kazunori; Nakatani, Seiichi

PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09324107	A2	19971216	JP 1996-146284	19960607
PRAI JP 1996-146284		19960607		

AB The compn. comprises (A) 100 parts **elec. conductive** compn. contg. a thermosetting **resin**, 2-65% binder contg. a curing agent, and 35-98% **elec. conductive** powders and (B) <300 parts solvent with soly. parameter (.delta.S) satisfying the following formula:|.delta.S - .delta.C| >1.5 (.delta.C = soly. parameter of the curing agent). The compn. shows good storage stability and its viscosity can be easily controlled before use.

L59 ANSWER 27 OF 27 HCAPLUS COPYRIGHT 2003 ACS
AN 1980:524622 HCAPLUS
DN 93:124622
TI Etching of metal layer on a hybrid integrated **circuit substrate**
IN **Suzuki, Takeshi**
PA Toko Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 2 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 55041758	A2	19800324	JP 1978-115327	19780920
JP 63021359	B4	19880506		
PRAI JP 1978-115327		19780920		

AB In forming elec. interconnection on an Al substrate for a hybrid integrated circuit by etching, the etching of the metal layer (e.g. Cu) on the substrate is carried out with an etching soln. prepd. by adding H3PO4 and HOAc to an aq. HNO3 soln., and the exposed Al is chem. oxidized to form a nonconductor layer.

01/31/2003

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(c)2003 Japan Science and Tech Corp(JST)
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01/31/2003

Set	Items	Description
S1	15043	CIRCUIT?(1N)(SUBSTRATE? OR LAYER? OR FILM OR COAT?)
S2	744	INSULAT?(W)BASE? ?
S3	9973	(WIRING OR WIRE? ?)(2N)(LAYER? OR FILM OR COAT?)
S4	240644	(ELECTRICAL?)(W)(CONNECT? OR CONDUCTIV? OR INTERCONNECT? OR JOIN?)
S5	92600	EPOXY(W)RESIN OR BISPHENOL OR DIPHENYLOLMETHANE OR EPICHLOROHYDRIN OR EPOXIDE(W)RESINS OR EPOXY(W)COMPOUND? ? OR EPOXY(W)POLYMERS OR EPOXY(W)RESINS
S6	113	UNCURED(N)RESIN
S7	195	METAL(2N)COHESION
S8	8	AU=(TOMEKAWA S OR TOMEKAWA, S OR TOMEKAWA SATORU OR TOMEKAWA, SATORU)
S9	4461	AU=(YAMASHITA, Y OR YAMASHITA Y OR YAMASHITA, YOSHIHISA OR YAMASHITA YOSHIHISA)
S10	26450	AU=(SUZUKI, TAKESHI OR SUZUKI TAKESHI OR SUZUKI, T OR SUZUKI T)
S11	241	AU=(KAWAKITA, YOSHIHIRO OR KAWAKITA YOSHIHIRO OR KAWAKITA Y OR KAWAKITA, Y)
S12	18399	AU=(NAKAMURA T OR NAKAMURA, T OR NAKAMURA OR TADASHI OR NAKAMURA, TADASHI)
S13	4	S1 AND S2
S14	0	S1 AND S6
S15	0	S1 AND S7
S16	300	S1 AND S4
S17	4	S16 AND S5
S18	6	S16 AND S3
S19	126	S1 AND S5
S20	12	S19 AND CONDUCTOR? ?
S21	3	S19 AND S3
S22	153	S1 AND S3
S23	0	S16 AND GLASS(W)TRANSITION?
S24	7	S19 AND GLASS(W)TRANSITION?
S25	0	S22 AND GLASS(W)TRANSITION?
S26	25	S1 AND GLASS(W)TRANSITION?
S27	59	S16 AND CONDUCTOR? ?
S28	31	S22 AND CONDUCTOR? ?
S29	51	S13 OR S17 OR S18 OR S20 OR S21 OR S24 OR S26
S30	46	RD (unique items)
S31	46	S30 NOT PD>=20001206
S32	42	S30 NOT PY>=20001206
S33	49244	S8:S12
S34	82	(S27 OR S28) NOT (S13 OR S17 OR S18 OR S20 OR S21 OR S24 OR S26)
S35	71	RD (unique items)
S36	70	S35 NOT PY>=20001206
S37	3	S36 AND (S5 OR RESIN? ?)
S38	22	S36 AND S3
S39	49244	S33 NOT (S29 OR S37 OR S38)
S40	9	S39 AND S1
S41	179	S39 AND S5
S42	0	S41 AND S4
S43	0	S41 AND S3
S44	9	S40
S45	9	RD (unique items)

32/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6383886 INSPEC Abstract Number: B1999-12-0170J-016
Title: High density MLB using additive and build-up process
Author(s): Enomoto, R.; Asai, M.; Hirose, N.
Author Affiliation: Div. of Technol. Res., IBIDEN Co. Ltd., Gifu, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.399-404
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.399:HDUA;1-3
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: A new type of printed circuit board, a high density MLB (multi-**layered** printed **circuit** board), has been developed for the high density routing and high reliability substrate requirements of LSI packages. The new technology has photo-resolution capability for line/space patterns of 35 mu m/35 mu m and 80 mu m diameter via holes. A full additive method is applied for the patterning, to attain the multi-layer structure. The insulator is a unique and newly developed photo-imageable dielectric resin which has a **glass transition** of 200 degrees C, peel strength of 1.2 kg/cm and withstands 1000 cycles of thermal cycling. The insulator is composed of high heat resistant photo-sensitive epoxy and super-engineering plastic. This technology is suitable for direct chip attachment. This paper describes the characteristics of the new MLB.
Subfile: B

32/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6146904 INSPEC Abstract Number: B1999-03-2210D-009
Title: New low dielectric constant, high T/sub g/, printed **circuitry substrates**
Author(s): Bissell, R.; Conrad, J.; Holman, E.; Reichenbacher, P.
Author Affiliation: AlliedSignal Laminate Syst. Inc., LaCrosse, WI, USA
Conference Title: IPC Printed Circuits Expo '98. Proceedings of the Technical Conference p.1-5
Publisher: Inst. Interconnecting & Packaging Electron. Circuits, Northbrook, IL, USA
Publication Date: 1998 Country of Publication: USA 732 pp.
Material Identity Number: XX-1998-01648
Conference Title: Proceedings of IPC Printed Circuits EXPO '98
Conference Sponsor: Arizona Printed Circuits Assoc.; Chicagoland Circuits Assoc.; Michigan Printed Circuits Assoc.; et al
Conference Date: 26-30 April 1998 Conference Location: Long Beach, CA, USA
Language: English
Abstract: AlliedSignal has developed a new family of fiber glass reinforced substrates (FR408) using a specially formulated **epoxy resin** to achieve a robust combination of performance and processing

characteristics. These substrates are low dielectric constant (Dk or epsilon), low loss (Df or tan delta) laminates with high **glass transition** temperatures (T/sub g/) which allow standard FR4 PCB fabrication processes. Their electrical properties are relatively insensitive to frequency, making these materials suitable for demanding communications, computing, and instrument applications. This paper discusses these new technologies, presenting results of PCB fabrication techniques for these materials as well as the benefits to the end users. Other products which address these needs have proven to be more difficult to process than standard FR4 materials. Comparisons of fabrication techniques of this product to FR4 processes are made. End user requirements such as dielectric performance in the GHz frequency range are compared to industry standard products.

Subfile: B

32/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5658365 INSPEC Abstract Number: B9709-2210-006

Title: Reliability of high aspect ratio plated through holes (PTH) for advanced printed circuit board (PCB) packages

Author(s): Goval, D.; Azimi, H.; Kim Poh Chong; Mirng-Ji Lii
Author Affiliation: Intel Corp., Chandler, AZ, USA

Conference Title: 1997 IEEE International Reliability Physics Symposium Proceedings. 35th Annual (Cat. No.97CH35983) p.129-35
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA vi+384 pp.
ISBN: 0 7803 3575 9 Material Identity Number: XX97-00834
U.S. Copyright Clearance Center Code: 0 7803 3575 9/97/$10.00
Conference Title: 1997 IEEE International Reliability Physics Symposium Proceedings. 35th Annual
Conference Sponsor: IEEE Electron. Devices Soc.; IEEE Reliability Soc
Conference Date: 8-10 April 1997 Conference Location: Denver, CO, USA
Language: English

Abstract: A plated-through hole (PTH) in multi-**layer** printed **wiring** boards (PWB) is defined as "a hole in which **electrical connection** is made between internal or external conductive patterns, or both, by plating of metal on the wall of the hole". The recent trend to increase the packaging density at all levels has resulted in a significant increase in PWB **wiring layers** and in turn for PTH density in order to communicate between the **layers** of **circuitry**. The increase in overall PCB thickness, coupled to the decrease in PTH diameter makes the PTH integrity during the assembly process and subsequent field stresses one of the primary reliability concerns in PWB production and usage. Thermo-mechanical stresses mainly due to mismatch in out-of-plane (z-direction) coefficient of thermal expansion (CTE) between the PTH metal and the laminated material can result in the failure of the PTHs. Failure of a PTH constitutes an electrical discontinuity which may be caused by fracture of the plating material at the barrel, fracture at the land-barrel junction, or delamination of the plating from the PWB. This paper will discuss the reliability performance of the PTHs when subjected to T/C (Temperature Cycle) stresses. During the initial reliability stressing through 1000 T/C `B' (-55 to 125 degrees C) and T/C `C' (-65 to 150 degrees C) electrical opens were observed. Physical analysis showed that the opens were due to barrel cracking of the PTHs. Extensive mechanical modeling and experimental validation were used to suggest changes in the materials, process and design to eliminate barrel cracking in high aspect ratio PTHs. Results of these analyses will be discussed in detail.

01/31/2003

Subfile: B
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32/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5477987 INSPEC Abstract Number: B9702-0170J-108
Title: A high density substrate with buried bump interconnection technology (B/sup 2/it)
Author(s): Sato, Y.; Shibayama, K.; Hamano, H.; Fukuoka, Y.
Author Affiliation: PCB & Module Eng. Dept., Toshiba Corp., Kawasaki, Japan
Conference Title: Proceedings of the 9th International Microelectronics Conference p.345-9
Publisher: Microelectron. Soc, Tokyo, Japan
Publication Date: 1996 Country of Publication: Japan xv+418 pp.
Material Identity Number: XX96-01947
Conference Title: Proceedings of the 9th International Microelectronics Conference
Conference Sponsor: Microelectron. Soc.-Japan
Conference Date: 24-26 April 1996 Conference Location: Omiya, Japan
Language: English
Abstract: A new type of **substrate** (printed **circuit** board) utilizing buried bump interconnection technology (B/sup 2/it) is developed. The structure of the B/sup 2/it substrate is different from conventional PCBs and **electrical interconnection** between layers is performed by conductive bumps piercing insulation layers not by PTH (plated through hole). The manufacturing process is also unique and simple as bumps are formed by printing and interconnection between layers is formed by lamination without drilling and plating. The features of B/sup 2/it substrates include: (1) pads for assembly can be laid out on the via bump, so very high assembly density can be achieved; (2) conductive bumps can be laid on at random between every **layer**, so higher **wiring** density can be achieved and design rule restrictions decrease; (3) finer lines and spaces can be formed because no plating makes etching easier; (4) due to the good peel strength of copper foil, multiple reworks are possible unlike the conventional substrate; (5) existing equipment and materials can be used; (6) due to the above, very good cost performance is achieved. This paper reports the variable structure and process of B/sup 2/it substrate and its reliability including practical utilization.
Subfile: B

32/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

4958113 INSPEC Abstract Number: B9507-0170G-004
Title: Feasibility of some lead-free solder alloys as filler materials for z-axis adhesives
Author(s): Savolainen, P.; Kivilahti, J.
Author Affiliation: Dept. of Mater. Sci. & Eng., Helsinki Univ. of Technol., Espoo, Finland
Journal: Soldering & Surface Mount Technology no.20 p.10-12
Publication Date: May 1995 Country of Publication: UK
CODEN: SSMOEO ISSN: 0954-0911
Language: English
Abstract: Polyester connector strips were joined to polyimide substrates

with anisotropic **electrically conductive** adhesives. Copper **conductors** as well as Au/Ni-coated copper **conductors** were used on flexible circuits. The adhesives were composite materials consisting of heat curing, one-component **epoxy resin** and powdered ternary solder alloys: tin-bismuth-zinc, tin-indium-zinc and tin-zinc-aluminium. An adhesive filled with eutectic tin-bismuth alloy powder was used as reference. The effect of bonding parameters (e.g., temperature, dwell time and pressure) on contact resistance values was evaluated. The contact resistance values were measured for evaluating the reliability of adhesive joints during a 60 degrees C/95%RH test. Furthermore, the joint microstructures were examined with optical and scanning electron microscopy. The results showed that with the copper **conductors** the initial contact resistance values were lower than with the Au/Ni-coated copper **conductors** . The most reliable joints were produced with low melting filler alloys (with respect to bonding temperature) on bare copper metallisation. The most likely reason for failure of the Au/Ni-**coated circuits** was strong oxidation of locally exposed nickel in the presence of moisture.
Subfile: B

32/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03071503 INSPEC Abstract Number: B88012854
Title: Copper thick film conductors in **insulation based** integrated circuits
Author(s): Baartke, I.
Journal: Finommechanika - Mikrotechnika vol.25, no.4-5 p.109-114
Publication Date: April-May 1986 Country of Publication: Hungary
CODEN: FNMKAY ISSN: 0324-7007
Language: Hungarian
Abstract: The topic of thick film conductors is surveyed. Following the introduction, the construction and technology of thick film conductors is dealt with. Particular methods concerning copper conductors are emphasized. Different properties of copper wiring layers and traditional precious metal layer wiring systems are compared. The obtained data show that the possible advantages of the application of copper conductors have not yet been fully exploited.
Subfile: B

32/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

02688944 INSPEC Abstract Number: B86040536
Title: Passing the screen printing test
Author(s): Hobby, A.
Author Affiliation: DEK Printing Machines, Weymouth, UK
Journal: Electronics Manufacture & Test vol.5, no.1 p.39-40
Publication Date: Jan. 1986 Country of Publication: UK
CODEN: ELMTD5 ISSN: 0265-301X
Language: English
Abstract: The most common assembly technique for placing devices on to a PCB thick film or thin **film circuitry** is to deposit a precise quantity of solder on to the respective **conductor** pads, place by hand or, increasingly, automatically and then reflow the solder to achieve a successful joint. As has long been the case in the thick film hybrid

industry, the use of solder paste (a suspension of metal alloys held in a vehicle with various types of flux) deposited by screen printing techniques has proved to be the most cost effective method of placing controlled quantities of solder where required. While, in principle, the techniques of screening solder creams and **epoxy resins** are the same, special consideration must be given to the solder cream's properties.
Subfile: B

32/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

02550254 INSPEC Abstract Number: B85061537
Title: Engineering-grade thermoplastics enhance PC-board design options
Author(s): Ormond, T.
Journal: EDN vol.30, no.18 p.67-70
Publication Date: 8 Aug. 1985 Country of Publication: USA
CODEN: EDNSBH ISSN: 0012-7515
Language: English
Abstract: Used as printed-**circuit substrates**, injection-moldable thermoplastic materials promise higher design flexibility and lower costs than do epoxy/glass laminates (FR-4 boards) in some specialized high-volume applications. Although by no means a replacement for epoxy/glass laminates in traditional, rigid PC-board applications, nor for flexible circuits in applications that require components to be mounted on multiple planes, molded circuit boards let you satisfy specific styling and functional requirements. Molded circuit boards best suit high-frequency and high-temperature applications that have historically required specialized laminate structures. Today's engineering-grade thermoplastics are an economical alternative to expensive and hard-to process laminates like PTFE-glass with its low-loss dielectric properties, Triazine-glass with its high conductive-anodic-filament (CAF) resistance and polyimide glass with its high **glass-transition** temperature.
Subfile: B

32/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

02444077 INSPEC Abstract Number: B85028793
Title: Substrates for PTF circuits
Author(s): Martin, F.W.
Author Affiliation: ECMA, Mamaroneck, NY, USA
Journal: Circuits Manufacturing vol.24, no.9 p.78-86
Publication Date: Sept. 1984 Country of Publication: USA
CODEN: CMFGAF ISSN: 0009-7306
Language: English
Abstract: Choosing the most appropriate substrate for a polymer thick **film circuit** can appear very difficult because there is such a wide range of choices. And since the electrical characteristics are affected by printing the circuit on the substrate, the decision seems even more complicated. This paper will make the decision simpler by explaining the nature of the PTF-substrate interface and by offering selection criteria. A general rule to fall back on is that any laminate substrate suitable for PC board manufacturing is compatible with PTF processes. Secondly, two important factors to keep in mind are the **glass transition** temperature and thermal expansion.
Subfile: B

32/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

00957005 INSPEC Abstract Number: B76037714
Title: Screen pattern generation by lasers
Author(s): Sugiyama, H.; Muto, H.; Kouno, E.; Tamura, T.
Journal: Journal of the Japan Society of Precision Engineering vol.42, no.6 p.478-84
Publication Date: June 1976 Country of Publication: Japan
CODEN: JJPEAD ISSN: 0912-0289
Language: Japanese
Abstract: This paper describes screen pattern generation by Nd:YAG and Ar lasers. The screen is used in fabrication of thick film hybrid integrated circuits and consists of a stainless steel **wire** mesh **coated** with filler material. A focused laser beam removes the filler material without thermally damaging the stainless steel mesh. **Epoxy resin**, polyvinylydene chloride, polyvinylydene fluoride, polyvinyl alcohol and polyvinyl acetate were selected as the filler materials. They were experimented with and the results were observed. Further experiments were conducted for polyvinyl alcohol fillers which showed good laser machinability, in order to investigate the relation between laser power and pattern width. The screen patterns were generated on a mini-computer controlled XY table. Printed **conductor** patterns had good specifications, and results showed possibilities for practical applications. Connecting this system to CAD (Computer Aided Design) will further enhance its effectiveness.
Subfile: A B

32/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

00957003 INSPEC Abstract Number: B76037712
Title: Construction and application of thick-**film** hybrid **circuits**
Author(s): Hetherington, D.R.
Author Affiliation: Newmarket Transistors Ltd., Newmarket, UK
Journal: Elektronik Industrie vol.7, no.5 p.104-6
Publication Date: May 1976 Country of Publication: West Germany
CODEN: EKIDAT ISSN: 0374-3144
Language: German
Abstract: Gives a brief introduction and state-of-the-art survey. The main attraction is the wide resistor range (1 to 10/sup 9/ Ohm) of high precision (0.5%). Materials for these resistors and for **conductors** and suitable methods for mounting discrete passive components (e.g. tantalum capacitors) and active elements (transistors) are described. Typical applications in communications, biomedicine and entertainment electronics are briefly treated and illustrated. A comprehensive table, quoting various encapsulation techniques (low-melting glass, phenolic and **epoxy resins**, injection mouldings, hermetic seals in metal- and ceramic cans) and the appropriate sizes, relative costs, temperature ranges and typical cycle-approval tests is given.
Subfile: B

32/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

01/31/2003

00817716 INSPEC Abstract Number: B75037602
Title: Process for manufacturing a conductive film for a thin **film** integrated **circuit** device
Inventor(s): Sato, A.; Sato, S.
Assignee(s): Nippon Electric Co. Ltd
Patent Number: US 3869367 Issue Date: 750304
Application Date: 730103
Priority Appl. Number: JP 47-130072 Priority Appl. Date: 721227
Country of Publication: USA
Language: English
Abstract: The process consists in forming a film of a first high-conductivity metal on an **insulator base** plate; forming a diffusion preventing insulator film on the metal; and sputtering a second metal susceptible to anodic film forming oxidation onto the insulator film, which is of such thickness as to permit particles of the second metal to penetrate at a multiplicity of locations, while leaving intact a sufficient insulating film substantially to prevent the formation of an alloy of the first and second metals, whereby a composite film is produced having a specific conductivity higher than that of either metal.
Subfile: B

32/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

00049693 INSPEC Abstract Number: B69015029
Title: Multilayer printed circuit wiht soldered eyelets forming the sole means joining the same
Inventor(s): Baxter, E.E.
Assignee(s): Motorola Inc
Patent Number: US 3424854 Issue Date: 690128
Application Date: 670720
Priority Appl. Number: US 654933
Country of Publication: USA
Language: English
Abstract: This device is a multi-**layer circuit** having an **insulating base** with a first layer of printed circuitry mounted on it. An insulating layer covers the first layer of printed circuitry and has a second layer of printed circuitry disposed on it. A plurality of funnel shaped eyelets pass through one or both of the insulating layers and selectively engage the first and second layers of printed circuitry. The eyelets bind all the layers together to form the multilayer circuit.
Subfile: B

32/3,AB/14 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1776039 NTIS Accession Number: AD-D015 966/5
Wire Assembly for **Electrically Conductive** Circuits (Patent)
Schneider, W. T.
Department of the Navy, Washington, DC.
Corp. Source Codes: 001840000; 110050
Report No.: PAT-APPL-7-866 921; PATENT-5 250 753
Filed 10 Apr 92 patented 5 Oct 93 4p
Languages: English Document Type: Patent

Journal Announcement: GRAI9405
Supersedes PAT-APPL-7-866 921, AD-D015 535.
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of patent available Commissioner of Patents, Washington, DC 20231.
NTIS Prices: Not available NTIS
A wire assembly for **electrically conductive** circuits, the assembly comprising a circuit conductor **wire** having a **coating** of insulative material thereon, a shielding foil wrapped at least partially around the coating and having a leg portion extending outwardly from the coating, a shield conductor wire fixed to the shielding foil, and an insulative outer layer enclosing the shielding foil and the shield conductor wire.

32/3,AB/15 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1620567 NTIS Accession Number: N92-11139/2
Evaluation of Kapton Pyrolysis, Arc Tracking, and Arc Propagation on the Space Station Freedom (SSF) Solar Array Flexible Current Carrier (FCC) (Final Report)
Stueber, T. J.
Sverdrup Technology, Inc., Brook Park, OH.
Corp. Source Codes: 097910000; S6005601
Sponsor: National Aeronautics and Space Administration, Washington, DC.
Report No.: NAS 1.26:189056; E-6655; NASA-CR-189056
Nov 91 8p
Languages: English
Journal Announcement: GRAI9205; STAR3002
Presented at the 22ND Photovoltaic Specialists Conference, Las Vegas, Nv, 7-11 Oct. 1991; Sponsored by IEEE.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Recent studies involving the use of polyimide Kapton **coated wires** indicate that if a momentary electrical short circuit occurs between two wires, sufficient heating of the Kapton can occur to thermally char (pyrolyze) the Kapton. Such charred Kapton has sufficient **electrical conductivity** to create an arc which tracks down the wires and possibly propagates to adjoining wires. These studies prompted an investigation to ascertain the likelihood of the Kapton pyrolysis, arc tracking and propagation phenomena, and the magnitude of destruction conceivably inflicted on Space Station Freedom's (SSF) Flexible Current Carrier (FCC) for the photovoltaic array. The geometric layout of the FCC, having a planar-type orientation as opposed to bundles, may reduce the probability of sustaining an arc. An experimental investigation was conducted to simulate conditions under which an arc can occur on the FCC of SSF, and the consequences of arc initiation.

32/3,AB/16 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

1060113 NTIS Accession Number: AD-D010 475/2
One-Side Transducer Lead Connection
(Patent Application)

01/31/2003

Scott, W. R.
Department of the Navy, Washington, DC.
Corp. Source Codes: 001840000; 110050
Report No.: PAT-APPL-6-395 546
Filed 6 Jul 82 14p
Languages: English Document Type: Patent
Journal Announcement: GRAI8325
This Government-owned invention available for U.S. licensing and, possibly, for foreign licensing. Copy of application available NTIS. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
A transducer is provided having interconnections between a conductive member and one side of a heat sensitive piezoelectric substrate such as PVF2 to or from which electric signals flow. The interconnections are positioned on one side of the substrate with the opposite side having a metalization under the interconnection attachment positions and in a continuous region therebetween. The interconnection includes adhesive material such as epoxy disposed between and attaching an **electrically conductive** member to one side of the substrate and a single contiguous **electrically conductive** coating applied to adjacent portions of these two members to **electrically conductive** coating applied to adjacent portions of these two members to **electrically connect** them. Since both interconnections are positioned on one side of the substrate the transducer is adhesively fastenable to operational structure with a strong bond line, permits lead attachment after mounting and prevents lead shortout. Various electrode shapes, sizes and patterns may be constructed to allow power channeling and to produce focusing of the transducer signal.

32/3,AB/17 (Item 4 from file: 6)
DIALOG(R)File 6:NTIS

0466076 NTIS Accession Number: AD-786 525/6/XAB
Testing of Conformal Coating by Using a Thermomechanical Test Method to Measure the **Glass Transition** (Tg) Property
(Technical rept)
Knowles, K. F.
Army Missile Command Redstone Arsenal Ala Product Test and Failure Analysis Div
Corp. Source Codes: 407059
Sponsor: Army Materials and Mechanics Research Center, Watertown, Mass.
Report No.: QL-TR-74-1
Jun 74 62p
Journal Announcement: GRAI7425
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NTIS Prices: PC A04/MF A01
In the study a thermomechanical test method was used to measure the **glass transition** temperature of conformal coating materials. This physical property offered a quantitative measure of the thermal changes that occur in a conformal coating material after exposure to environmental conditions. The data obtained by this test method may be used as an aid in the quality evaluation of a conformal coating applied to printed wiring boards. (Author)

01/31/2003

32/3,AB/18 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05590026
E.I. No: EIP00065218934
Title: Reduction formation, Part 2
Author: Wolter, Andreas
Corporate Source: Photo Print Electronic GmbH, Schopfheim, Ger
Source: Printed Circuit Fabrication v 23 n 6 2000. 2 pp
Publication Year: 2000
CODEN: PCFAE6 ISSN: 0274-8096
Language: English
Abstract: The key to building up multiple microvia-**layer circuits** is the registration of the microvias and the **conductor** pattern of the microvia layers. In general, microvia layers are aligned with respect to the **conductor** pattern of the layer underneath. This is the only way to keep the microvia pads small and thus make optimum use of the space savings offered by the technology. However, the cumulative offset does not present any problems as long as the structure does not contain any elements which have to be well-aligned with respect to all the layers at the same time. Some techniques on how to maintain registration of buildup microvias are discussed.

32/3,AB/19 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05504892
E.I. No: EIP00035088040
Title: Polymer thick film resistor with a dual curing system
Author: Hwang, Hui-min; Chung, Chia-Tin; Su, Te-Yeu; Wang, Wun-Ku; Wang, Hsin-Herng; Lin, Bin-Yuan
Corporate Source: Union Chemical Lab Industrial Technology Research Inst, Hsinchu, Taiwan
Conference Title: Proceedings of the 1999 International Symposium on Microelectronics
Conference Location: Chicago, IL, USA Conference Date: 19991026-19991028
E.I. Conference No.: 56143
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3906 1999. p 489-492
Publication Year: 1999
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: Embedding polymer passive component is an inexpensive means of burying passive components into organic substrate. The polymer pastes for passive components contain several kinds of conductive powder and additives. This investigation presents a novel approach to manufacture environmental and process friendly polymer based resistor materials by developing a screen printable solventless resin system. The study included the following: polymerization kinetics, cure profile, conductivity during cure and **glass transition** temperature. The polymer thick film resistor (PTFR) materials are showing excellent performance that includes dimensional stability, UV hardenable resistant traces. The benefits incurred are achieved by combining a conductive carbon black with a low viscosity, fast gel times elevated temperature combined with a long storage life time and solventless **epoxy resin** formulation. This process

is purely additive, non-polluting and not produce waste. How the process affects the electrical properties, screen printability, and cost of the composite at the loading required to achieve the desired conductivity level must be considered to properly select a conductive carbon black. The pastes can be printed on the 400 mesh count screens, and tested from the polymer composition with a sheet resistivity of paste ranging from 10 Omega /square to 10 M Omega /square when the surface of resist traces is hardened by UV radiation and bulk polymerized by heat. (Author abstract) 8 Refs.

32/3,AB/20 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05504884
E.I. No: EIP00035088032
Title: Characteristics and reliability of no-flow underfills for solder bumped flip chips on low cost substrates
Author: Lau, John H.; Chang, Chris; Chen, Chih-Chiang
Corporate Source: Express Packaging Systems, Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the 1999 International Symposium on Microelectronics
Conference Location: Chicago, IL, USA Conference Date: 19991026-19991028
E.I. Conference No.: 56143
Source: Proceedings of SPIE - The International Society for Optical Engineering v 3906 1999. p 439-449
Publication Year: 1999
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: Solder bumped flip chips on low cost substrates with three different epoxy-based no-clean flux liquid-like no-flow underfills are presented in this study. Important material and process parameters such as curing temperature and time, thermal coefficient of expansion, storage modulus, loss modulus, tan delta , **glass transition** temperature, moisture uptake, solder reflow, and post curing are discussed. Also, cross-sections are examined for a better understanding of the effects of these no-flow underfill materials on the interconnects of the flip chip assemblies. Shear and thermal-cycling tests and results of these flip chip assemblies are reported and analyzed. (Author abstract) 29 Refs.

32/3,AB/21 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04955262
E.I. No: EIP98024091367
Title: SiLK polymer coating with low dielectric constant and high thermal stability for ULSI interlayer dielectric
Author: Townsend, P.H.; Martin, S.J.; Godschalx, J.; Romer, D.R.; Smith, D.W. Jr.; Castillo, D.; DeVries, R.; Buske, G.; Rondan, N.; Froelicher, S.; Marshall, J.; Shaffer, E.O.; Im, J.-H.
Corporate Source: Dow Chemical Co, Midland, MI, USA
Conference Title: Proceedings of the 1997 MRS Spring Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19970401-19970404
E.I. Conference No.: 46963
Source: Low-Dielectric Constant Materials III Materials Research Society Symposium Proceedings v 476 1997. MRS, Warrendale, PA, USA. p 9-17
Publication Year: 1997

CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: A novel polymer was developed for use as a thin film dielectric in the interconnect structure of high density integrated **circuits**. The **coating** is applied to the substrate as an oligomeric solution, SiLK, using conventional spin coating equipment and produces highly uniform films after curing at 400 degree C to 450 degree C. The oligomeric solution, with a viscosity of ca. 30 cPs, is readily handled on standard thin film coating equipment. The properties of the cured films are designed to permit integration with current interlayer dielectric processes. The dielectric constant of cured SiLK has been measured at 2.65. The refractive index in both the in-plane and out-plane directions is 1.63. 5 Refs.

32/3,AB/22 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04471824
E.I. No: EIP96083284983
Title: PBGA wire bonding development
Author: Shu, William K.
Corporate Source: VLSI Technology, Inc
Conference Title: Proceedings of the 1996 IEEE 46th Electronic Components & Technology Conference, ECTC
Conference Location: Orlando, FL, USA Conference Date: 19960528-19960531
E.I. Conference No.: 45119
Source: Proceedings - Electronic Components and Technology Conference 1996. p 219-225
Publication Year: 1996
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: In a PBGA package, the existing of a **glass transition** temperature of 170approx.215 degree C for PCB substrate puts an upper ceiling to the usable wire bond temperature. The low thermal conductivity of PCB substrate and the need for a thicker material make fine pad pitch wire bonding even more difficult to do. To compensate for the limitation in thermal energy, high frequency thermo-sonic bonding was proposed and successfully demonstrated for fine pad pitch wire bonding. Of the four major bonding parameters investigated, bond force appeared to be the most important control factor for ball size and ball shear force optimization. By using ball size, ball shear force, and ball shear stress, respectively as objective functions, a minimum ball size of Xs equals 2.6 mil, Ys equals 2.7 mil, a maximum ball shear force of 41.9 g, and a maximum ball shear stress of 5.6 g/mil**2 were predicted. Tradeoffs may be necessary for a given bonding application. (Author abstract) 5 Refs.

32/3,AB/23 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04234063
E.I. No: EIP95082825620
Title: Evaluation of epoxy underfill materials for use in 'chip-on-board' method of packaging silicon integrated circuits
Author: Park, C.E.; Raju, V.R.; Bair, H.E.; Han, B.J.
Corporate Source: Pohang Univ of Science and Technology, Pohang, S Korea
Conference Title: Proceedings of the 53rd Annual Technical Conference. Part 2 (of 3)

Conference Location: Boston, MA, USA Conference Date: 19950507-19950511
E.I. Conference No.: 43446
Source: Annual Technical Conference - ANTEC, Conference Proceedings v 2 1995. Soc of Plastics Engineers, Brookfield, CT, USA. p 2871-2876
Publication Year: 1995
CODEN: ACPED4
Language: English
Abstract: In flip-chip technology, the gap between the chip and the substrate is underfilled with highly filled **epoxy resins** to coupled the chip and substrate mechanically. Physical properties of epoxy underfill materials such as **glass transition** temperature (Tg) and coefficient of thermal expansion (CTE) were examined. In order to obtain void-free flip-chip assemblies, the flow behavior of epoxy underfill materials was investigated. The adhesion strength between solder ball and epoxy underfill materials was measured using a novel method. The effect of moisture and thermal shock on the adhesion strength were also studied. (Author abstract) 5 Refs.

32/3,AB/24 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04085847
E.I. No: EIP95022592502
Title: Basismaterialien fuer das 21. Jahrhundert
Title: Substrate materials for the 21st century
Author: Forcier, R.
Source: Galvanotechnik v 85 n 11 Nov 1994. p 3830-3835
Publication Year: 1994
CODEN: GVTKAY ISSN: 0016-4232
Language: English; French; German
Abstract: Higher packaging densities and miniaturization-reduction of weight and/or volume are the driving forces behind circuit assembly developments for the future. Examples of these trends are MCM, PCMCIA cards, high density thin-film multilayers and similar packages with fine-line structure micro-holes and Direct Chip Attachment. Suitable substrates for such developments will be ultra-thin copper laminates based on multi-functional resins, using materials with low dielectric constants and high T//g and these are discussed. A trend away from glass fibre mats towards random non-woven felts is discernible as is also the use of adhesive-free films of polyimide, PTFE and LPC (liquid film polymer). (Translated author abstract)

32/3,AB/25 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02653244
E.I. Monthly No: EI8810096866
Title: THICKFILM CIRCUITS WITH GaAsIC: PROTOTYPE MANUFACTURING OF DIGITAL HYBRID CIRCUITS WITH WIREBONDED GaAsIC.
Author: Jorgensen, Tom
Source: Elektronikcentralen (Report) ECR 215 May 1988 69p
Publication Year: 1988
CODEN: ELKRDN
Language: English
Abstract: Mounting of GaAs IC's for high frequencies above 1 GHz has successfully been performed with thermocompression wedge/wedge wire bonding of the IC's to multilayer thickfilm circuits with filled vias and printed

resistors. The influence of the bonding wires on the circuit performance was reduced by bonding at least two wires per IC-terminal, and further by developing a two-layer substrate technique with 'put-through holes' in the top substrate for the GaAs chip which is mounted on the bottom or ground substrate. This has resulted in bonding wires between GaAs chip and substrate as short as 0. 3 mm. Silver filled glue was used for the die attachment and **electrical connection** of ceramic chip capacitors and SMA-connector pins. The mounted substrate was glued to a heat sink and surrounded by a connector holder frame for the connectors. (Author abstract)

32/3,AB/26 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02559743
E.I. Monthly No: EIM8804-023094
Title: EFFECT OF MOISTURE IN HOLE WALL PULL-AWAY FOR MULTI-LEVEL PACKAGES.
Author: Susko, R. A.; Susko, J. R.; Livingston, E. D.; Marsh, L. L.; Tomek, R. E.
Corporate Source: IBM Corp, Endicott, NY, USA
Conference Title: Proceedings of the Symposium on Multilevel Metallization, Interconnection, and Contact Technologies. (Part of the 169th Meeting of the Electrochemical Society.)
Conference Location: San Diego, CA, USA Conference Date: 19861021
E.I. Conference No.: 10835
Source: Proceedings - The Electrochemical Society v 87-4. Publ by Electrochemical Soc Inc, Pennington, NJ, USA p 152-172
Publication Year: 1987
CODEN: PESODO ISSN: 0161-6374
Language: English
Abstract: A study of the 'hole wall pull-away' phenomenon observed throughout the multi-**layer circuit** board industry was performed. Many process variables were altered in order to create the areas of metal delamination. Based on observations from those tests, a model is proposed for 'hole wall pull-away' in multi-level electronic packages and is discussed. Alternate models are also presented. The effect of moisture absorption on a typical epoxy composite and the deposited metal **electrical interconnection** is shown to have the capability of initiating 'hole wall pull-away'. Theoretical values for laminate swelling/shrinkage, based on experimental diffusion/solubility experiments, correlate well with observed regions of metal/epoxy delamination. (Edited author abstract) 7 refs.

32/3,AB/27 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02523856
E.I. Monthly No: EIM8801-003835
Title: HIGH-DENSITY MULTILAYER HYBRID CIRCUITS MADE WITH POLYMER INSULATING LAYERS (POLYHIC'S).
Author: Shiflett, C. C.; Buchholz, D. B.; Faudskar, C. C.; Small, R. D.; Markham, J. L.
Corporate Source: AT&T Bell Lab
Conference Title: Proceedings of the 1986 International Symposium on Microelectronics.
Conference Location: Atlanta, GA, USA Conference Date: 19861006

E.I. Conference No.: 10579
Source: Publ by Int Soc for Hybrid Microelectronics, Reston, VA, USA p 481-486
Publication Year: 1986
ISBN: 0-930815-16-5
Language: English
Abstract: An extension of the Hybrid Integrated Circuit technology, designated POLYHIC's, has been developed by adding alternate layers of polymer and metal to conventional Hybrid Integrated Circuits. The polymer formulation was developed within AT&T to provide the required combination of lithographic, thermal, and mechanical properties. The cured polymer has a **glass transition** temperature of about 150 DEGREE C, and will withstand soldering temperatures without damage. The dielectric constant of 3. 6 and a polymer thickness of 50 micrometers allows fabrication of controlled impedance lines. The multiple **layers** of **circuity** produce high packing densities and simplify circuit layout because of the high interconnectability of the structure. Design rules and fabrication procedures have been developed. Accelerated environmental tests have been performed, including temperature-humidity-bias, elevated temperature, and temperature cycling. 3 refs.

32/3,AB/28 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01963051
E.I. Monthly No: EI8604035062
E.I. Yearly No: EI86117654
Title: THERMOPLASTIC SUBSTRATES.
Author: Hastie, William M.
Corporate Source: Circuits Manufacturing, Boston, MA, USA
Source: Circuits Manufacturing v 25 n 10 Oct 1985 p 31-32
Publication Year: 1985
CODEN: CMFGAF
Language: ENGLISH
Abstract: Experts see tremendous potential for injection molded board designs including recessed circuitry and 3-D features such as component supports, structural ribs, fasteners and battery clips. Fully 3-D circuitry can be printed onto product housings. The thermoplastic materials themselves also offer performance advantages for the end user: high dielectric strength, high resistivity, low dissipation factor, high **glass transition** temperature and an inherent flame retardancy. Injection molded printed circuit boards offered by several manufacturers are introduced.

32/3,AB/29 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01848629
E.I. Monthly No: EIM8501-002898
Title: PREPARATION OF POLYMER THICK FILM PASTES.
Author: Leppavuori, S.; Pienimaa, S.; Muilu, M.
Corporate Source: Univ of Oulu, Microelectronics Lab, Oulu, Finl
Conference Title: Proceedings - 4th European Hybrid Microelectronics Conference.
Conference Location: Copenhagen, Den Conference Date: 19830518
E.I. Conference No.: 05693
Source: Proceedings - European Hybrid Microelectronics Conference 4th.

Available from Int Soc for Hybrid Microelectronics, Montgomery, AL, USA p 275-282
Publication Year: 1983
CODEN: PEMCDQ
Language: English
Abstract: Preparation of polymer thick film pastes demands a lot of experimental study of the effects of the paste components on the properties of the pastes. Different polymer pastes were made using thermosetting polymer, ammonia catalyzed phenol-cresole or epoxy. In the resistive pastes the resistive part was treated carbon black; in the dielectric pastes the fillers were silica and aluminum oxide; and in the **conductor** pastes the functional phase was silver flakes. The pastes were satisfactory on phenolic paper and epoxy paper boards. 11 refs.

32/3,AB/30 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01848600
E.I. Monthly No: EIM8501-002869
Title: PROCEEDINGS - 4TH EUROPEAN HYBRID MICROELECTRONICS CONFERENCE.
Author: Anon
Conference Title: Proceedings - 4th European Hybrid Microelectronics Conference.
Conference Location: Copenhagen, Den Conference Date: 19830518
E.I. Conference No.: 05693
Source: Proceedings - European Hybrid Microelectronics Conference 4th. Available from Int Soc for Hybrid Microelectronics, Montgomery, AL, USA 563p
Publication Year: 1983
CODEN: PEMCDQ
Language: English
Abstract: Proceedings includes 60 papers, of which two are in the form of abstracts only and one is given as a summary only. The papers are subdivided into ten sessions dealing with properties of thick-film **conductors** and resistors, component attachment, assembly-encapsulation-packaging, sensors, non-noble and polymer pastes, manufacturing, microwave applications, various applications as well as thermal design and reliability prediction. Topics considered include: automotive electronics, **epoxy resins**, color printing, sensors, laser beam applications, military aircraft equipment, active and microwave filters, fiber optics, strip lines, optical communication equipment, resonators, humidity control, soldering, and computer-aided design and manufacturing.

32/3,AB/31 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00141056
E.I. Monthly No: EI71X027921
Title: Auto voltage regulator typical of new uses for thick **film circuits**.
Author: KNOX, G. H.
Source: Assembly Engineering v 13 n 7 July 1970 p 36-9
Publication Year: 1970
CODEN: AYEGA ISSN: 0004-5063
Language: ENGLISH
Abstract: Hybrid thick film microelectronics already is firmly

established as an inhouse production technology in the computer industry where it was developed. A thick **film circuit** consists of an **insulative base**, usually a ceramic such as alumina, on which the electricallyconductive paths of the circuit and the resistors are screen printed and then fixed by firing in a furnace. This article describes some of the manufacturing operations in the production of the hybrid voltage regulator for the 1970 model year, with special emplasis on the assembly processes and equipment.

32/3,AB/32 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01240975 AAD9229603
FORMULATION, DEVELOPMENT, AND CHARACTERIZATION OF MAGNETIC PASTES AND EPOXIES FOR THICK FILM INDUCTORS (FERRITE EPOXIES)
Author: RIAHI KASHANI, MOHAMMAD MANSOUR
Degree: PH.D.
Year: 1992
Corporate Source/Institution: VIRGINIA POLYTECHNIC INSTITUTE AND STATE UNIVERSITY (0247)
Source: VOLUME 53/05-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 2467. 262 PAGES

Inductors and transformers constitute two important magnetic components in RF and power hybrids electronic **circuitry**. Thick **film** inductors have been subject of extensive research in recent years because they significantly reduce the weight and size, and increase the frequency of operation of electronic circuits. The research work in this dissertation is aimed at the formulation of thick film ferrite pastes and ferrite epoxies and the design, construction, and evaluation of thick film spiral inductors. Wideband characterization (DC-2GHz) of ferrite pastes, ferrite epoxies, and ferrite substrates is performed using two techniques. These techniques are based on current image and transmission line (coaxial cavity) concepts for low (DC-100MHz) and high (50MHz-2GHz) frequency regions, respectively. They are used to evaluate the permeability spectra of formulated and commercially available thick film magnetic materials in respective frequency ranges.

A method to numerically calculate the inductance of thick film circular spiral inductors based on modeling the spiral as concentric circles is presented. A novel method for fine as well as coarse tuning of thick film inductors is also introduced. The tunable inductors are constructed using formulated ferrite epoxies and magnetic cores. The method of analysis of variance is used to investigate the variation significance of tunable inductors. Finally, chemical and mechanical properties of developed magnetic materials are discussed. The studied properties include, **glass transition** temperature, degradation temperature, thermal coefficient of expansion, adhesion, particle-size distribution and particle densification, grain size, and compositional constituents of the magnetic materials.

32/3,AB/33 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02293011 JICST ACCESSION NUMBER: 95A0153269 FILE SEGMENT: JICST-E
New Multi-layer Boards Incorporating IVH: HITAVIA.
TSUYAMA KOICHI (1); KIDA AKINARI (1); OTSUKA KAZUHISA (1); NAKASO AKISHI (1); OGINO HARUO (2); TAMURA YOSHIHIRO (2)

(1) Hitachi Chem. Co., Ltd., Res. & Dev. Adm. Group; (2) Hitachi Chem. Co., Ltd., Ind. Laminates Div.
Hitachi Kasei Tekunikaru Repoto(Hitachi Chemical Technical Report), 1995, NO.24, PAGE.17-20, FIG.5, TBL.1, REF.5
JOURNAL NUMBER: X0860AAB ISSN NO: 0288-8793
UNIVERSAL DECIMAL CLASSIFICATION: 671.315.616 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The miniaturization of high performance electronic equipment requires thinner printed wiring boards(PWBs) with higher wiring density. The requirement is causing the spread of the interstitial via hole(IVH), in which only the necessary portions between **wiring layers** are connected with non-through holes. This has led to the development of new multi-layer IVH-incorporating PWBs (HITAVIA), employing the copper foil with the newly developed B-stage epoxy film. The technical key point is to perforate the foil, prior to the lamination of the copper foil on the inner **circuit layer**, thereby forming IVHs. It is possible to make the insulation layers thinner and to form smaller diameter IVH, since no glass cloth is used as the reinforcement. Because both IVHs and through-holes, formed after lamination, are made conductive simultaneously in the single plating step, the process reduces the number of steps involved and enables thinning of the outer conductive layer, which facilitates micro-fine wiring through etching (five lines between pins). This technology is effective to reduce the manufacting cost of PWBs with IVHs. (author abst.)

32/3,AB/34 (Item 2 from file: 94)

01159384 JICST ACCESSION NUMBER: 91A0080045 FILE SEGMENT: JICST-E
Printed wiring boards. Copper-clad laminates for printed wiring boards.
AOKI MASAMITSU (1); KUROKAWA NORIO (1)
(1) Toshiba Chemical Corp.
Toshiba Rebyu(Toshiba Review), 1990, VOL.45,NO.12, PAGE.980-982, FIG.5, REF.2
JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper discusses the development of high-**glass-transition**-temperature (Tg) laminate and thin-mass laminate with inner-**layer circuits**, which are major challenges for the laminate industry. A description is given of a new, high-performance high-Tg laminate and thin-multilayer application. This laminate is unique among other high-Tg laminates. (author abst.)

32/3,AB/35 (Item 3 from file: 94)

00711853 JICST ACCESSION NUMBER: 88A0601123 FILE SEGMENT: JICST-E
Multilayer copper-lined laminated board incorporating the high **glass transition** temperature glass epoxy inner **layer**

circuit.
TAKEGUCHI KAZUNORI (1)
(1) Rishokogyo Kagiken
Denshi Zairyo(Electronic Parts and Materials), 1988, VOL.27,NO.10, PAGE.72-76, FIG.12, TBL.1
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

32/3,AB/36 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00230367 JICST ACCESSION NUMBER: 86A0222822 FILE SEGMENT: JICST-E
Special article: All about electronic materials currently required. High-function glass materials.
SUZUKI YOSHIRO (1)
(1) Asahi Glass Co., Ltd.
Kogyo Zairyo(Engineering Materials), 1986, VOL.34,NO.4, PAGE.122-128, FIG.5, TBL.7, REF.15
JOURNAL NUMBER: F0172AAZ ISSN NO: 0452-2834 CODEN: KZAIA
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5 681.7.068:535.3 666.1/.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

32/3,AB/37 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2229495 H.W. WILSON RECORD NUMBER: BAST00073582
Qualification of a spin apply, photodefinable polymer for packaging of automotive circuits
Wyant, J. L; Schuckert, C. C
Solid State Technology v. 43 no11 (Nov. 2000) p. 125-30
DOCUMENT TYPE: Feature Article ISSN: 0038-111X

ABSTRACT: Several spin-apply polyimide coatings are examined for use in the packaging of automotive **circuits**. These **coatings** can be used as a stress buffer passivation layer for improved device reliability or as dielectric and passivation layers in bond pad redistribution circuits for flip-chip packaging. A high **glass-transition**-temperature photodefinable polyimide was chosen for both applications due to its good chemical resistance and its good adhesion to various compounds and itself.

32/3,AB/38 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14165533 PASCAL No.: 99-0363546
Polyquinoline/bismaleimide blends as low-dielectric constant materials
Electrochemical processing in ULSI fabrication I and Interconnect and contact metallization : materials, processes, and reliability : San Diego CA, 4-5 May 1998

HARI SINGH NALWA; SUZUKI M; TAKAHASHI A; KAGEYAMA A
ANDRICACOS PC, ed; DUKOVIC JO, ed; MATHAD GS, ed; OLESZEK GM, ed; RATHORE HS, ed; REIDSEMA SIMPSON C, ed
Hitachi Research Laboratory, Hitachi Ltd., 7-1-1 Ohmika-cho, Hitachi City, Ibaraki 319-1292, Japan; Hitachi Chemical Co. Ltd., 9-25-4 Shibaura, Minato-ku, Tokyo 108, Japan
Electrochemical Society. Electrodeposition Division, Pennington NJ, United States.; Electrochemical Society. Electronics Division, Pennington NJ, United States.; Electrochemical Society. Dielectric Science and Technology, United States.
Electrochemical processing in ULSI fabrication. Symposium, 1Interconnect and contact metallization. Symposium (San Diego CA USA) 1998-05-04
Journal: Proceedings - Electrochemical society, 1999, 6 135-144
Language: English
Low-dielectric constant (K) materials have attracted much attention in the field of microelectronics packaging. Currently a number of low dielectric constant polymers have been reported with K in the range of 2.2 to 3.0, however, hardly any polymer satisfies all desired material requirements. Polyquinolines are thermoplastic polymers which show low dielectric constant, high thermal stability, good mechanical strength and low moisture absorption. We have blended a polyquinoline designated as PQ-100 with a bismaleimide in order to improve physical properties for microelectronics packaging applications. We have prepared transparent, tough polyquinoline/ bismaleimide blend thin films containing 5 to 60 weight % bismaleimide contents as low-dielectric constant interlayer materials for multilevel interconnections. The effect of bismaleimide loading and curing conditions on dielectric, dynamic mechanical and thermal stability properties of polyquinoline/bismaleimide thermoset blends was studied. By the incorporation of the bismaleimide, the blend thin films showed higher **glass transition** temperature up to 360 Degree C. The dielectric, thermal and mechanical properties of polyquinoline/bismaleimide blend thin films are discussed.

32/3,AB/39 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

13318825 PASCAL No.: 98-0043825
High temp, high speed
COPPENS D
AlliedSignal Laminate Systems, La Crosse WI, United States
Journal: Printed Circuit Fabrication, 1997, 20 (12) 18-20
Language: English
Before the introduction of high-temperature FR-4 materials to the electronics industry, non-polyimide applications that required higher thermal performance than standard FR-4 would often use BT/epoxy. Although blends such as these were originally formulated with higher electrical performance, these materials also had a higher **glass transition** temperature than standard FR-4 grades. BT/epoxy blends filled what was once a relatively small niche in the market. The industry was in effect making do with a material that was neither easy to process nor had FR-4 economics. When high-temperature FR-4 materials started to prove themselves in the early to mid '90s, they quickly replaced BT/epoxy blends in many of these higher temperature applications.

32/3,AB/40 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

01/31/2003

09833257 PASCAL No.: 92-0035586
Conduction paths and mechanisms in FR-4 epoxy/glass composite printed wiring boards
TAKAHASHI K M
AT&T Bell Laboratories, Murray Hill NJ 07974, USA
Journal: Journal of the Electrochemical Society, 1991, 138 (6) 1587-1593
Language: English

32/3,AB/41 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

02977520 NEDO-90-950331; EDB-91-011144
Title: Wiring board material HHR'' of hybrid heat resistant **epoxy resin** for high density mounting
Original Title: Komitsudo jissoyo koseino tainetsu epoxy haisenban zairyo HHR''
Author(s): Takahama, T.; Kikuchi, T.; Oka, S.; Nakajima, H. (Mitsubishi Electric Corp., Tokyo (Japan))
Source: Kino Zairyo (Japan) v 10:9. Coden: KIZAE ISSN: 0286-4835
Publication Date: 5 Aug 1990
p 11-19
Language: In Japanese
Abstract: Wiring board material HHR'' of hybride heat resistant **epoxy resin** for high density mounting was developed to respond to high densification on print wiring board and this paper reported the features. Exclusive **epoxy resin** is widely used for electronic equipments, but there are some problems such as deformation by soldering, blister in internal layer or fault of through hole **conductor** by multilayer structure owing to the larger thermal expansion of Z direction. For these reasons, polyimide wiring board is used for multilayer wiring board for high density mounting but this resin has weak points such as higher cost and long time and high temperature setting. This time development is based on the bonding at molecular level of multi functional **epoxy resin** of superior thermal resistance and thermal plastic resin of superior flexibility. Print wiring board made by this material has balanced properties of high thermal resistance, low moisture absorption and low thermal expansion, and is optimal for high density mounting. 5 refs., 15 figs., 1 tab.

32/3,AB/42 (Item 2 from file: 103)
DIALOG(R)File 103:Energy SciTec

01818977 INS-86-025938; EDB-86-142850
Title: Nuclear static eliminators halt airborne contamination and enhance personnel safety
Author(s): Edelmann, G.F.; Regan, J.T.
Affiliation: Nelco Products, Inc., Fullerton, CA
Source: Chem. Process. (Chicago) (United States) v 48:12. Coden: CHPCA
Publication Date: Oct 1985
p 122-123
Language: English
Abstract: In January 1984, Nelco Products, Inc. opened a new plant in Fullerton, CA to produce fiberglass/epoxy sheet stock which is used to manufacture single-sided, double-sided and multi-**layer** printed

circuit boards (PCB) for electronic and telecommunications apparatus. The process for making the PCB core material begins with woven fiberglass fabric which passes through a series of metal take-up and tensioning rollers, and is then immersed in and impregnated with an equivalent weight of **epoxy resin**. Shortly after startup, the plant encountered quality control and safety problems due to electrostatic charges that commonly occur when processing non-**conductors** such as fiberglass plastics and paper given serious consideration until the plant had been operating for about six months and continued to have quality and safety problems due to static charges. The engineers decided to try a bar-type nuclear static eliminator containing polonium 210 (Po-210) whose emissions create both negative and positive air ions. The nuclear-powered device is available only on an annual renewable lease, because the normal useful life is one year, and the US Nuclear Regulatory Commission requires a leak test each 12 months. A fresh bar is shipped to the lessee at the end of the 12-month period, and the old one is returned to the lessor. The nuclear-powered static eliminators have improved the quality of the PCB core material since the fiberglass cloth is practically free of any dirt or dust before it enters the resin-impregnating bath. Furthermore, the operators no longer complain about electrical shocks.

01/31/2003

(Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03503004 INSPEC Abstract Number: B89075436
Title: New assembly technology 'micro-bump bonding method'
Author(s): Fujimoto, H.; Hatada, K.; Ochi, T.; Ishida, Y.; Okamoto, I.; Suzuki, T.; Sakiyama, T.; Hidaka, K.
Author Affiliation: Semicond. Res. Center, Osaka, Japan
Journal: National Technical Report vol.35, no.3 p.95-102
Publication Date: June 1989 Country of Publication: Japan
CODEN: NTROAV ISSN: 0028-0291
Language: Japanese
Abstract: A new LSI-chip bonding method named the 'micro-bump bonding method' has been developed. This makes possible micron-order direct bonding between LSI electrodes and **circuit substrate** electrodes. The technology consists of three elements: an LSI chip with bumps, a **circuit substrate** and light-setting insulating **resin**. The LSI chip is attached by the adhesive force of the light-setting insulation **resin**. The **electrical connection** between the bumps of the LSI chip and the **conductor** pattern of the substrate is accomplished by means of the shrinkage stress induced in the light-setting **resin**. The electrical characteristics and reliability were evaluated. This technology has been applied to thermal heads and an LED printer head.
Subfile: B

37/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

02444122 INSPEC Abstract Number: B85028838
Title: Multi-chip module using copper thick film
Author(s): Ikehata, M.; Iguchi, Y.; Arao, Y.; Shibata, I.; Nihei, K.
Author Affiliation: Res. Lab., OKI Electr. Ind. Co., Ltd., Tokyo, Japan
Journal: International Journal for Hybrid Microelectronics vol.7, no.2 p.35-9
Publication Date: June 1984 Country of Publication: USA
CODEN: IMICDJ ISSN: 0277-8270
Language: English
Abstract: An LED multi-chip module mounting 225 LED chips on a copper thick film substrate was developed. DuPont 9923 and 9924 copper pastes for copper thick film **conductors** and DuPont 4275 and 4575 pastes for the dielectric were used. These were compared with respect to inter-layer insulation, adhesion, substrate bowing, wire-bond pull strength and electrical resistance, and die-bond characteristics. As a result of these studies, a combination of DuPont 9923 and 4575 was selected and a crossover two-layer substrate was fabricated. 225 LED chips were mounted on the crossover two-layer substrate. The LED chips were die-bonded, in the n-side down configuration, on the second **conductor** layer with conductive **resin**, and anode-electrodes were connected to the first **conductor layer** by Al **wires**. This module can drive any of the 225 LED chips on the substrate by selection of the corresponding pair of signal lines. The new module offered the possibility of mounting bare chips on a copper thick film.
Subfile: B

37/3,AB/3 (Item 1 from file: 103)
DIALOG(R)File 103:Energy SciTec

01/31/2003

03589600 NEDO-93-921124; EDB-94-005566
Title: Electro conductive plastic compound containing stainless steel fiber for electro static discahrge, 'SUSTEC'
Original Title: Stainless fiber juten seidenki taisakuyo dodensei compound 'SUSTEC'
Author(s): Sakamoto, R.; Komori, E. (Kawasaki Steel Techno Research Corp., Tokyo (Japan))
Source: Kawasaki Seitetsu Giho (Kawasaki Steelmaking Technical Report) (Japan) v 25:2. Coden: KWSGBZ ISSN: 0368-7236
Publication Date: Jun 1993
p 69-71
Language: Japanese
Abstract: An outline is given on a color electro-conductive stainless steel fiber packed compound which has been developed for its application to parts for static electricity elimination used in the field of semiconductors or peripheral equipment of electronic **circuit substrate**. This article is manufactured by such method that a compound is prepared by dispersing stainless steel fibers and a characteristics improver into thermoplastic **resin** of polypropylene or polystyrene as base material using an original technique and then the compound is subjected to injection molding. The molding has homogeneous volume and surface resistivity and uniform appearance that no packed fibers are seen. It generates no dust due to friction in its use; it has excellent stability against oxidation and undergoes no change in electric conductivity with the lapse of time. The developed product shows a uniform surface resistance of 10[sup 3]-10[sup 4] ohm and moldings of various shapes show 10[sup 4]-10[sup 5] ohm. There are three items of elastic-, impact resistant and heat-resistant grades. Its applications cover heat-resistant trays to be used in the process of heat treatment of semiconductors, multi-purpose trays for shipping, **electrically conductive** containers and racks for the system stock room of electronic parts. 3 figs., 3 tabs.

01/31/2003

38/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5204663 INSPEC Abstract Number: B9604-2210D-017
Title: Versatile, low cost, multilayer ceramic board on metal core
Author(s): Kumar, A.H.; Prabhu, A.N.; Thaler, B.J.
Author Affiliation: David Sarnoff Res. Center, Princeton, NJ, USA
Conference Title: Proceedings 1995 International Conference on Multichip Modules (SPIE Vol.2575) p.100-7
Publisher: ISHM-Microelectron. Soc, Reston, VA, USA
Publication Date: 1995 Country of Publication: USA 572 pp.
ISBN: 0 930815 42 4 Material Identity Number: XX95-01257
Conference Title: Proceedings 1995 International Conference on Multichip Modules (SPIE Vol.2575)
Conference Sponsor: ISHM-Microelectron. Soc.; Int. Electron. Packaging Soc.; Electron. Ind. Assoc.; Components, Packaging, Manuf. Technol. Soc. IEEE
Conference Date: 19-21 April 1995 Conference Location: Denver, CO, USA
Language: English
Abstract: A low cost method for manufacturing multilayer ceramic boards on a metal core is described in this paper. The projected low cost is due to the ease of process control, high yields, and the choice of thick film silver **conductors** to enable fast firing in air ambient. The metal core completely suppresses lateral shrinkage during sintering. It also enables the processing of large, thin substrates, thereby increasing productivity. In use, the metal core can serve as a heat spreader, ground plane, and package reinforcement. Both single and double-sided LTCC-M circuit boards have been fabricated on Cu-Mo-Cu metal cores. A crystallizable glass yielding a glass-ceramic expansion-matched to the metal core with low dielectric constant and low loss characteristics has been developed for this application. Additional thin **film wiring** (MCM-C/D) structures can be formed on these substrates.
Subfile: B

38/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4794360 INSPEC Abstract Number: B9411-2220J-015
Title: Qualification and validation of a process for thin film MCM fabrication
Author(s): Palleau, J.; Jourdain, D.; Oberlin, J.C.; Alaimo, M.; Clarisse, C.; Templier, F.; Argoud, G.; Aubert, D.; Beudon, M.; Bouzid, M.J.; Laviale, D.; Torres, J.
Author Affiliation: CNET, Meylan, France
p.224-31
Publisher: Int. Soc. Hybrid Microelectron, Versailles, France
Publication Date: 1993 Country of Publication: France vii+499 pp.
Conference Title: Proceedings of 9th ISHM-European Hybrid Microelectronics Conference
Conference Date: 2-4 June 1993 Conference Location: Nice, France
Language: English
Abstract: Thin film MCM technology is believed the ultimate solution for applications where performance is required. However costs have to be improved to make these solutions attractive in high volume productions. This work describes the systematic qualification and validation approach followed to perfect the very aggressive thin film technology developed in

our laboratory. Silicon has been chosen as the network base while the interconnect network is formed with polymer as dielectric and copper as **conductor** . The intrinsic performances of these materials represent a first criteria for choice. But the study shows how essential it is to check the evolution of these performances all along the assembling processes involving thermal and chemical treatments cycles. The mastering of the interfacial effects appear a particularly critical point to optimize the compatibility between the materials and between the processes used for their deposition, their curing and patterning. Advanced physical characterizations have been performed as well as electrical measurements made on technology representative test patterns and test vehicles. Finally, as a result of this systematic approach, substrates have been assembled and tested, with a functional yield of 50%. Increasing performances for VLSI and ULSI circuits are demanding new technological solutions for interconnection at the circuit level as well as at the inter-circuit level in view of fitting with high input/output numbers and high clock frequency values. This tendency explains increasing Research and Development efforts on Multichip Modules (MCM) technologies. Among MCM solutions, the thin film technology seems alone able to translate the high speed available on chips to fast MCM, placing chips as closely as possible to reduce chip-to-chip travel time. Thin film technology is also the ultimate solution to handle the increasing numbers of I/O per chip, reducing by an order of magnitude the number of **wiring layers** as compared to thick-film solutions.
Subfile: B

38/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

04397212 INSPEC Abstract Number: B9306-2220J-007
Title: Basic hybrid IC technology must adapt to dense mounting
Author(s): Ono, Y.
Author Affiliation: Fujitsu General Ltd., Tokyo, Japan
Journal: JEE (Journal of Electronic Engineering) vol.30, no.315 p. 54-7
Publication Date: March 1993 Country of Publication: Japan
CODEN: JEENDL ISSN: 0385-4507
Language: English
Abstract: Mounting densities in printed circuit boards continue to improve with widespread use of surface mounting technology (SMT) and progress in board manufacturing techniques for fine, multi-**layer conductor wiring** . The latest performance enhancements for parts-mounting machines significantly lower the mounting costs for printed circuits boards. Against this backdrop, the applications for conventional hybrid ICs with ceramic substrates have contracted. To improve this situation, hybrid IC (HIC) manufacturers are working to raise these devices from the level of standard components to the subsystem level.
Subfile: B

38/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

04353395 INSPEC Abstract Number: B9304-0170J-026
Title: Repair of thin **film wiring** with laser-assisted processes
Author(s): Wassick, T.A.
Author Affiliation: IBM E. Fishkill, Hopewell Junction, NY, USA

Conference Title: 1992 Proceedings. 42nd Electronic Components and Technology Conference (Cat. No.92CH3056-9) p.759-62
Publisher: IEEE, New York, NY, USA
Publication Date: 1992 Country of Publication: USA xviii+1095 pp.
ISBN: 0 7803 0167 6
U.S. Copyright Clearance Center Code: 0569 5503/92/0000-0759$03.00
Conference Sponsor: IEEE; Electron. Ind. Assoc
Conference Date: 18-20 May 1992 Conference Location: San Diego, CA, USA
Language: English
Abstract: The ability to repair defective circuit elements on the high end packaging components being built by IBM for the System/390 is important in meeting yield and reliability targets. A number of laser-based technologies have been developed at IBM, establishing the capability to modify fine line circuit patterns on a range of packaging materials. The ability to control the laser/material interaction with the ability to successfully modify the circuit without adversely affecting the integrity of the dielectric is discussed. Removal of unwanted **conductors** is done with a computer-controlled, excimer-laser micromachining system operating at 308 nm. New **conductor** segments are created through the laser chemical vapor deposition of gold from the pyrolytic decomposition of dimethyl-Au-trifluoroacetylacetonate. The applications of these techniques to IBM's thin film packaging are described, with specific focus on the two technologies introduced for the manufacture of high end, thin film packaging products.
Subfile: B

38/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04200149 INSPEC Abstract Number: B9209-2220E-001
Title: Laser processes for repair of thin **film wiring**
Author(s): Wassick, A.
Author Affiliation: IBM East Fishkill, Hopwell Junction, NY, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1598 p.141-8
Publication Date: 1991 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
U.S. Copyright Clearance Center Code: 0 8194 0729 1/91/$4.00
Conference Title: Lasers in Microelectronic Manufacturing
Conference Sponsor: SPIE
Conference Date: 10-11 Sept. 1991 Conference Location: San Jose, CA, USA
Language: English
Abstract: Several laser-based technologies have been developed at IBM, establishing the capability to modify fine line circuit patterns on inorganic (glasses and ceramics) and organic (polymers) dielectric packaging materials. These modification techniques, either to repair defects created during the manufacturing process or to restructure the circuit for design and performance reasons, can be achieved with the proper control of the laser conditions. This ability to control the laser/material interaction, with the goal of successfully modifying the circuit without adversely affecting the integrity of the dielectric is discussed. The applications of these techniques to IBM's thin film packaging are described, with specific focus on the two technologies recently introduced for the manufacture of East Fishkill's new high end packaging products. Removal of unwanted **conductors** is done with computer controlled, excimer laser micromachining system operating at 308 nm. New **conductor** paths are created through the laser chemical vapor

deposition (LCVD) of gold from the pyrolytic decomposition of dimethyl-Au-trifluoroacetylacetonate. Connections are made by scanning a focussed argon ion laser across the surface in the presence of a gas-phase ambient of the organometallic. Both of these technologies are now fully established on manufacturing production lines.
Subfile: B

38/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

03546039 INSPEC Abstract Number: B90007497
Title: Biased humidity testing of copper thick-**film** ceramic printed **wiring** boards
Author(s): Kitano, P.T.
Author Affiliation: Scrantom Eng. Inc., Costa Mesa, CA, USA
Conference Title: IEPS. Proceedings of the Technical Conference. Ninth Annual International Electronics Packaging Conference p.3-16 vol.1
Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA
Publication Date: 1989 Country of Publication: USA 2 vol. 1391 pp.
Conference Date: 11-13 Sept. 1989 Conference Location: San Diego, CA, USA
Language: English
Abstract: Standard nitrogen-fireable thick-film materials were used to fabricate biased humidity test coupons. Various layering configurations were used to evaluate the system's basic insulation properties. Standard 3-**conductor** (SEM B format) and 7-**conductor** (SEM D format) Multilayer Interconnect Boards (MIBs) were also tested to evaluate the insulation resistance of actual products. Surface shorting, especially between exposed copper pads, is highly probable during biased humidity testing. Conductive surface contamination which develops on the circuit during chamber exposure must be removed before final insulation resistance measurements are taken. Copper thick-**film** printed **circuit** boards can meet biased humidity insulation requirements of the Navsea Thick-Film Multilayer Performance Specification Hash 6228507 when surface contamination is removed.
Subfile: B

38/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

03037663 INSPEC Abstract Number: B88001301
Title: An investigation of the parameters affecting the wire bonding characteristics of a doped thick film gold
Author(s): Twerski, I.M.; Richardson, W.W.
Author Affiliation: Engelhard Corp., East Newark, NJ, USA
Conference Title: Proceedings of the 1986 International Symposium on Microelectronics p.72-5
Publisher: Int. Soc. Hybrid Microelectron, Reston, VA, USA
Publication Date: 1986 Country of Publication: USA 915 pp.
Conference Sponsor: Int. Soc. Hybrid Microelectron.
Conference Date: 6-8 Oct. 1986 Conference Location: Atlanta, GA, USA
Language: English
Abstract: Discusses the characteristics of a new mixed bonded aluminium **wire** bondable thick **film** gold ink. Multilayer compatibility, wire bonding 'windows', and multiple firing characteristics are described. The state of the art vehicle system used in this ink yields printing properties superior to those of older pastes. This material is Engelhard

Gold **Conductor** Paste A4935. This material is prepared following proprietary procedures including the addition of dopants to achieve the desired properties. The films produced by this paste have properties similar to those of the standard gold **conductors** available with the addition of aluminium wire bondability.
Subfile: B

38/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

02689090 INSPEC Abstract Number: B86041388, C86035819
Title: CAD for the small firm: from circuit diagram to printed **circuit** board **film**
Journal: CAE Journal no.2 p.34-6
Publication Date: March-April 1986 Country of Publication: West Germany
CODEN: CAJOED ISSN: 0724-9985
Language: German
Abstract: The low cost CAD software package CADdy for printed circuit board design enabling the entire sequence from circuit diagram to printed **wiring** board **film** to be effected at a personal computer workstation is introduced. Use of symbols reduces time spent in circuit representation, and parts lists can be called up immediately. Design data can be stored on diskette or transmitted to a larger computer, and diagrams at several levels are drawn by plotter. The software package covers component packing density, multilayer technique, **conductor** spacing and size, sensitive component location, and other aspects. Component placement, **conductor** routing, design refinement, and drawing output, are described.
Subfile: B C

38/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

02444122 INSPEC Abstract Number: B85028838
Title: Multi-chip module using copper thick film
Author(s): Ikehata, M.; Iguchi, Y.; Arao, Y.; Shibata, I.; Nihei, K.
Author Affiliation: Res. Lab., OKI Electr. Ind. Co., Ltd., Tokyo, Japan
Journal: International Journal for Hybrid Microelectronics vol.7, no.2 p.35-9
Publication Date: June 1984 Country of Publication: USA
CODEN: IMICDJ ISSN: 0277-8270
Language: English
Abstract: An LED multi-chip module mounting 225 LED chips on a copper thick film substrate was developed. DuPont 9923 and 9924 copper pastes for copper thick film **conductors** and DuPont 4275 and 4575 pastes for the dielectric were used. These were compared with respect to inter-layer insulation, adhesion, substrate bowing, wire-bond pull strength and electrical resistance, and die-bond characteristics. As a result of these studies, a combination of DuPont 9923 and 4575 was selected and a crossover two-layer substrate was fabricated. 225 LED chips were mounted on the crossover two-layer substrate. The LED chips were die-bonded, in the n-side down configuration, on the second **conductor** layer with conductive resin, and anode-electrodes were connected to the first **conductor layer** by Al **wires** . This module can drive any of the 225 LED chips on the substrate by selection of the corresponding pair of signal lines. The new module offered the possibility of mounting bare chips on a copper thick film.

01/31/2003

Subfile: B

38/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

02032764 INSPEC Abstract Number: B83023978
Title: Manufacturing technology for high ohms per square films
Author(s): Linder, J.F.; Lee, M.A.; Magee, G.
Author Affiliation: Technol. Support Div., Hughes Aircraft Co., El Segundo, CA, USA
Journal: International Journal for Hybrid Microelectronics vol.5, no.2 p.189-96
Publication Date: Nov. 1982 Country of Publication: USA
CODEN: IMICDJ ISSN: 0277-8270
Conference Title: 1982 International Microelectronics Symposium
Conference Date: 15-17 Nov. 1982 Conference Location: Reno, NV, USA
Language: English
Abstract: A process for fabricating substrates with a high sheet resistivity film for hybrid circuits applications was developed. These substrates have a 2 to 3 kilo ohm per square cermet resistive layer covered by a palladium diffusion barrier layer, topped by a thick gold **conductor layer** suitable for **wire** bonding. The technique for patterning these substrates by photolithography was demonstrated. The formulation of the cermet layer, its deposition and annealing processes were optimized to achieve a low TCR and long term stability. A pilot production of such substrates was demonstrated in one of Hughes Aircraft Company's production facilities.
Subfile: B

38/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

01913801 INSPEC Abstract Number: B82045921
Title: Contamination of multilayer printed wiring boards-a case study
Author(s): Henesian, A.
Author Affiliation: Lockheed Missiles & Space Co., Sunnyvale, CA, USA
Journal: Journal of Environmental Sciences vol.25, no.2 p.31-4
Publication Date: March-April 1982 Country of Publication: USA
CODEN: JEVSAG ISSN: 0022-0906
Language: English
Abstract: Multilayer printed wiring boards (PWBs) are three-dimensional interconnection assemblies which are used to interconnect modern miniature electrical parts in the smallest possible space. Narrow **conductor** traces, narrow **conductor** spacings, and many **wiring** or **circuit layers** place stringent requirements for electrical insulation resistance, which is provided by the heterogeneous glass-polymer matrix of the PWB. Multilayer PWBs have been used in satellite electronic equipment since 1966 and have exhibited an extraordinary history of failure-free performance. However, a sudden and unexpected showing of insulation resistance anomalies prompted an in-depth investigation into all the materials and processes used in production. The author summarizes the analysis and testing performed to ferret out the cause of failures, the derivation of a more effective cleaning process, and positive actions needed to maintain electrical insulation for the most sensitive electronic equipments.
Subfile: B

38/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

01833639 INSPEC Abstract Number: B82020011
Title: Ultrasonic aluminum wire bonding to copper **conductors**
Author(s): Pitt, V.A.; Needes, C.R.S.; Johnson, R.W.
Author Affiliation: Photo Products Dept., E.I. du Pont de Nemours & Co., Inc., Wilmington, DE, USA
Journal: Insulation/Circuits vol.27, no.12 p.51-5
Publication Date: Nov. 1981 Country of Publication: USA
CODEN: ISCUBF ISSN: 0020-4544
Language: English
Abstract: Demonstrates the feasibility of making reliable ultrasonic aluminium wire bonds to thick **film** copper compositions. **Wire** deformation, although on the borderline of the range for ultrasonic wedge bonds, is within Military Specification 883 that calls for deformation to be maintained within 1.2 to 3.0 times of the original wire diameter. Bond failure occurs exclusively by wire breaks. Minimum pull strengths, in excess of the Military Specification of 2.5 grams for 25 mu m (1 mil) and 3.0 grams for 31.75 mu m (1.25 mil) wires, were achieved for all bonds following storage at elevated temperatures for 1000 to 2000 hours and thermal cycling between minus 55 degrees C and 150 degrees C. The system is extremely stable: little or no diffusion occurs during high temperature storage up to 250 degrees C and no electrochemical corrosion occurs during storage at high humidity.
Subfile: B

38/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

01495744 INSPEC Abstract Number: B80018749
Title: Alloyed thick-film gold **conductor** for high-reliability high-yield wire bonding
Author(s): Horowitz, S.J.; Felten, J.J.; Gerry, D.J.
Author Affiliation: Electronic Materials Div., E.I. du Pont de Nemours & Co. Inc., Niagara Falls, NY, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.CHMT-2, no.4 p.460-6
Publication Date: Dec. 1979 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
Conference Title: Proceedings of the 29th Electronic Components Conference
Conference Sponsor: IEEE
Conference Date: 14-16 May 1979 Conference Location: Cherry Hill, NJ, USA
Language: English
Abstract: Describes a new reduced thickness ('thin') thick-film gold **conductor**, developed to give the high reliability and high yield required for both ultrasonic aluminum wire bonding and automatic thermosonic gold wire bonding interconnection methods. In applications requiring ultrasonic aluminum wire bonding and elevated temperature burn-in or life tests, solid-state reactions occur at **wire** bond/thick-**film** interfaces that degrade bond integrity. The changes in these reactions and in interconnection performance when an alloying element is added to the reduced thickness thick-film **conductor** is focused on. The effect of elevated temperature storage on wire bond resistance is also determined. The reduced thickness alloyed gold is shown to have greater

bonding latitude than the conventional alloyed metallization in the formation of ultrasonic aluminum wire bonds. The differences in ultrasonic aluminum wire bond performance of the gold **conductors** were explored through scanning electron microscopy and X-ray analysis of the interface metallurgy. Mechanistic aspects are described.
Subfile: B

38/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

01495692 INSPEC Abstract Number: B80018694
Title: New Multiwire meets the challenge of interconnecting chip-carriers (for LSI)
Author(s): Messner, G.; Page Burr, R.
Author Affiliation: PCK Technol. Div. of Kollmorgen Corp., Glen Cove, NY, USA
Journal: Electronics vol.52, no.26 p.117-21
Publication Date: 20 Dec. 1979 Country of Publication: USA
CODEN: ELECAD ISSN: 0883-4989
Language: English
Abstract: Multiwire, a technique for automatically 'writing' insulated wires onto an adhesive-**coated** printed-**circuit** board, has been highly successful as an alternative to the more complex and expensive multilayer board approach. Originally designed to interconnect 14- and 16-pin dual in-line packages, it has now been upgraded to face the increasing interconnection densities that will be needed for the new, small chip-carriers housing large- and very large-scale integrated circuits. Multiwire is based on a new computer-controlled machine, the T-14. It has a redesigned wiring head that can put down finer wires on a much smaller grid, 25 to 18 mils, than the original system's 50-mil grid. The T-14 can thus place a **layer** of **wires** with a density of 80 inches of **conductor** per square inch for its normally used 6.3-mil wire and 100 inches of **conductor** per square inch for 4-mil wire. By comparison, the older system has a maximum density of 40 inches of 6.3-mil wire per square inch per **layer** of **wiring**.
Subfile: B

38/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

01409052 INSPEC Abstract Number: B79042260
Title: Alloyed thick film gold **conductor** for high reliability-high yield wire bonding
Author(s): Felten, J.J.; Gerry, D.J.; Horowitz, S.J.
Author Affiliation: Electronic Materials Div., E.I. du Pont de Nemours & Co. Inc., Niagara Falls, NY, USA
Conference Title: Proceedings of the 29th Electronic Components Conference p.179-86
Publisher: IEEE, New York, NY, USA
Publication Date: 1979 Country of Publication: USA ix+422 pp.
Conference Sponsor: IEEE
Conference Date: 14-16 May 1979 Conference Location: Cherry Hill, NJ, USA
Language: English
Abstract: In applications requiring ultrasonic Al wire bonding and elevated temperature burn-in or life tests, solid state reactions at **wire** bond/thick **film** interfaces degrade bond integrity. This

paper focuses on the changes in these reactions and in interconnection performance when an alloying element is added to the reduced thickness film **conductor**.
Subfile: B

38/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

01268250 INSPEC Abstract Number: B78049511
Title: Aluminum **wire** to thick-**film** connections for high-temperature operation
Author(s): Palmer, D.W.; Ganyard, F.P.
Author Affiliation: Sandia Labs., Albuquerque, NM, USA
Journal: IEEE Transactions on Components, Hybrids, and Manufacturing Technology vol.CHMT-1, no.3 p.219-22
Publication Date: Sept. 1978 Country of Publication: USA
CODEN: ITTEDR ISSN: 0148-6411
Conference Title: Proceedings of the 28th Electronic Components Conference
Conference Sponsor: IEEE
Conference Date: 24-26 April 1978 Conference Location: Anaheim, CA, USA
Language: English
Abstract: Hybrid microcircuits in geothermal instrumentation must operate from room temperature to 300 degrees C. Bond failure occurred during operation of initial geothermal circuits due to intermetallic growth at the aluminum wire-to-gold **conductor** interface. To remedy this problem, two wire bonding techniques have been qualified in high-temperature aging tests: ultrasonic bonding of aluminum wire directly to modified fritless gold **conductor** inks (DuPont 9910, AVX 3520, and TFS A328) and insertion of a 1 mil diffusion barrier pad between the thick film and the aluminum wire. Both systems allow 100-1000 h operation at 3000 degrees C.
Subfile: B

38/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

01167369 INSPEC Abstract Number: B78014363
Title: Ultrasonic aluminum wire bonding and lead/indium soldering to gold alloy thick film **conductors**-performance and failure mechanism
Author(s): Horowitz, S.J.; Gerry, D.J.; Cote, R.E.
Author Affiliation: Electronic Materials Div., E.I. du Pont de Nemours and Co. Inc., Niagara Falls, NY, USA
Conference Title: ATFA 77 p.227-35
Publisher: IEEE, New York, NY, USA
Publication Date: 1977 Country of Publication: USA viii+345 pp.
Conference Sponsor: IEEE
Conference Date: 27-29 Sept. 1977 Conference Location: Los Angeles, CA, USA
Language: English
Abstract: Compares the ultrasonic aluminum wire bonding performance of a state-of-the-art thick film gold **conductor** and similar materials containing small amounts of an alloying element. It is shown that for extended storage (to 2000 hours) at temperatures between 125 degrees C and 175 degrees C the added element causes a change in failure mode and an increase in pull strength. Wire bonds on unalloyed controls exhibit mean pull strengths of 3-4 grams and fail at the thick **film**

conductor/aluminum **wire** interface. Wire bonds on alloyed **conductors** exhibit mean pull strengths of 5.5-6.5 grams and fail at the aluminum wire heels. In the latter case, decrease in pull strength is found to be consistent with the loss in strength of the wire due to annealing.
Subfile: B

38/3,AB/18 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0684988 NTIS Accession Number: AD-A050 742/6/XAB
Periodic Surface Acoustic Wave Electromagnetic Transducers
Szabo, T. L. ; Frost, H. M. ; Sethares, J. C.
Rome Air Development Center Hanscom AFB Mass Deputy for Electronic Technology
Corp. Source Codes: 409761
Report No.: RADC/ETR-78-0044
13 Aug 76 16p
Document Type: Journal article
Journal Announcement: GRAI7811
Pub. in IEEE Transactions on Sonics and Ultrasonics, vSU-24 n6 p393-406 Nov 77. Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Previous work on surface acoustic wave (SAW) electromagnetic transducers (EMT) is briefly and selectively (but for the first time, extensively) reviewed, followed with presentation of our own new developments. Emphasis in the review is placed on transducer **conductor** pattern fabrication methods and unapodized transducer theory and experiment. Included in the first category are **wire**, thin-**film**, printed-**circuit**, and flat-cable technologies. Our own prior model for a meander-line flat-**conductor** transducer is presented here for the first time in its entirety - from calculation of the dynamic magnetic fields of the EMT **conductors** and a subsequent normal mode analysis to expressions of transducer efficiency for various matching conditions. New theoretical results systematically incorporate grating as well as meander-line **conductor** patterns, harmonic generation, and an eddy current impedance that decreases with transducer lift-off from a metal sample.

38/3,AB/19 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

0623042 NTIS Accession Number: AD-485 386/7/XAB
Bonding of Component Leads and Wire **Conductors** to Nafi Thin **Film Circuits** Using Hand Soldering Techniques
(Final rept. for 1965)
Slone, O. W. ; Shank, W. M.
Naval Avionics Facility Indianapolis Ind
Corp. Source Codes: 247950
Report No.: NAFI-TR-748
8 Jun 66 12p
Journal Announcement: GRAI7713
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located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
The results of tests on the hand soldering of component leads and wire **conductors** to thin **film circuits** are presented in this report. (Author)

38/3,AB/20 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04177506
E.I. No: EIP95062731067
Title: **Wire** bonded thick **film** silver multilayer for under-the-hood automotive applications
Author: Aday, Jon; Johnson, R. Wayne; Evans, John L.; Romanczuk, Chris
Corporate Source: Auburn Univ, Auburn, AL, USA
Source: International Journal of Microcircuits and Electronic Packaging v 17 n 3 Third Quarte 1994. p 302-311
Publication Year: 1994
CODEN: IMICDJ ISSN: 1063-1674
Language: English
Abstract: Thick film silver **conductors** provide a cost effective approach for the fabrication of automotive hybrids. Two prototype, underhood automotive hybrids have been fabricated using chip and wire assembly. A thick film dielectric was printed to prevent silver migration between the **conductor** traces. For assembly, gold wire was thermosonically bonded directly to the thick film silver pads. The exposed silver bond pads were encapsulated at the same time liquid encapsulant was applied to protect the semiconductor die. One of the hybrid circuits has been successfully demonstrated in test cars and the other hybrid circuit has passed electrical testing. Thermal cycling high temperature storage, boiling water, and biased humidity storage tests have been performed on the test structures to evaluate the integrity of the fabrication process. (Author abstract) 5 Refs.

38/3,AB/21 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02678226
E.I. Monthly No: EIM8811-058509
Title: COMPUTER-AIDED DESIGN OF MULTI-LAYER THICK-**FILM** HYBRID **CIRCUITS**.
Author: Osborne, M. R.; Green, R.
Corporate Source: Cent for Industrial Microelectronic Applications, Aust
Conference Title: Microelectronics Conference, VLSI 1987: Electronics - The Enabling Technologies. Preprints of Papers.
Conference Location: Melbourne, Aust Conference Date: 19870408
E.I. Conference No.: 11638
Source: National Conference Publication - Institution of Engineers, Australia 87/5. Publ by Inst of Engineers, Australia, Aust p 131-132
Publication Year: 1987
CODEN: NPIEDX ISSN: 0313-6922 ISBN: 0-85825-346-1
Language: English
Abstract: Despite advances in monolithic VLSI, hybrid thick-film remains an important technology particularly where a number of disparate characteristics are required in one package. In order to match the I/O pin densities of VLSI devices that might be mounted on a hybrid circuit, more than the usual two **wiring layers** are frequently needed. One of

the major problems with multilayer design is that to provide a reasonably flat surface for the printing of the second and subsequent **conductor** patterns, a fill-in dielectric layer must be provided for each **conductor** level. This means that for every **conductor** layer, two dielectric layers must be designed. This paper describes the way that the R. M. I. T. C. A. D. tools have been adapted to allow the design of multi-layer hybrid thick-**film circuits** with the automatic generation of the required dielectric layers. The way that this technique is used to design a five layer hybrid is described and a set of design rules for multi-layer hybrid thick-**film circuit** design are presented. (Author abstract) 2 refs.

38/3,AB/22 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02074878 JICST ACCESSION NUMBER: 94A0470207 FILE SEGMENT: JICST-E
Nearing MCM age.(4).Specified classification of MCM-L, C, D structures.(2).
HONDA SUSUMU (1); HATADA KENZO (2); HORINO NAOHARU (3)
(1) Esuvshivraboratori; (2) Matsushita Electr. Ind. Co., Ltd.; (3) Oki Electr. Ind. Co., Ltd.
Erekutoronikusu Jisso Gijutsu(Electronic Packaging Technology), 1994, VOL.10,NO.6, PAGE.105-109, FIG.6, TBL.1
JOURNAL NUMBER: L0322AAG ISSN NO: 0911-3053
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Trend in titled thema is outlined mainly on MCM-D using a thin **film** multilayer **wiring** technology. Characteristics of ceramic, Cu, Al, Si substrates and a base substrate through diamond thin film which is excellent in thermal conductivity are described. Development trends of polyimide with 3.3 dielectric constants, SiO2 (dielectric constant of 3.9), and other low dielectric-constant thin film material are introduced, and their applications as well as main properties such as high speed performance, **wiring** density, internal **layer conductor** resistance are discussed.

01/31/2003

45/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05909681 Genuine Article#: XG014 Number of References: 45
Title: Excellence of gate oxide integrity in metal-oxide-semiconductor large-scale-integrated circuits based on P-/P- thin-film epitaxial silicon wafers (ABSTRACT AVAILABLE)
Author(s): Shimizu H (REPRINT) ; Sugino Y; **Suzuki T**; Kiyota S; Nagasawa K; Fujita M; Takeda K; Isomae S
Corporate Source: HITACHI LTD,SEMICOND & INTEGRATED CIRCUITS DIV/KODAIRA/TOKYO 187/JAPAN/ (REPRINT); HITACHI LTD,KOFU OPERAT SEMICOND & INTEGRATED CIRCUITS DIV/YAMANASHI 40001//JAPAN/; HITACHI LTD,CENT RES LAB/KOKUBUNJI/TOKYO 185/JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1997, V36, N5A (MAY), P2565-2570
ISSN: 0021-4922 Publication date: 19970500
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: The substitution of Czochralski (CZ)-silicon (Si) wafers into p(-)(n(-))/p(-)(n(-)) (p(-) or n(-) layer on p(-) or n(-) Si substrate: resistivity of approximately 100 m Omega m) thin-film epitaxial Si wafers used as starting materials has been investigated with respect to application to metal-oxide-semiconductor (MOS) large-scale-integrated circuits (LSIs). The optimum epitaxial layer (p(-)/p(-) structure) thickness for MOS-LSIs was determined to be approximately 1 mu m from the viewpoints of gate oxide integrity (GOI) improvement and cost effectiveness. With increasing epitaxial layer thickness from 0.1 to 0.3 mu m, the oxide defect density was greatly reduced and leveled off at approximately 1/30 that of a CZ-Si layer if the layer thickness is above 0.3 mu m. This is because microdefects in CZ-Si represented by crystal originated particles (COP) which cause weak spots in the gate oxide layer are covered by an excellent Si epitaxial layer on the OZ-Si surface. The p(-)/p(-) thin epitaxial structure results in very controlled resistivity for electrically active regions in the device, resulting in a lower cost of growth.

45/3,AB/2 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

03205518 Genuine Article#: NM746 Number of References: 0
(NO REFS KEYED)
Title: FLEXIBLE MULTILAYER PRINTED-CIRCUIT BOARD DESIGN BY USE OF SPRINT CAD-SYSTEM (Abstract Available)
Author(s): SOGA O; HOSHIKAWA E; **NAKAMURA T**; OKUGAWA K
Journal: SHARP TECHNICAL JOURNAL, 1994, N58 (MAY), P45-48
ISSN: 0285-0362
Language: JAPANESE Document Type: ARTICLE
Abstract: In the camera unit of liquid crystal camcorder, we have designed a new flexible multi-**layer** printed **circuit** board by use of ''SPRINT'' which is one of the CAD systems for the printed circuit board.

By adopting the new flexible multi-**layer** printed **circuit** board to the camera unit, it is not necessary to use connectors between the printed circuit boards. Further it is useful for making a small size device, because the inner space of devices can be

used effectively.

With using the SPRINT, we have shorten the development period by 35% in comparison with the conventional developing method.
This paper describes an application of SPRINT and a structure of the flexible multi-**layer** printed **circuit** board. These have realized small size, light weight, and thin thickness in the liquid crystal camcorder.

45/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01128943 JICST ACCESSION NUMBER: 90A0606007 FILE SEGMENT: JICST-E
New porcelain-enamelled-steel board with improved surface condition.
ITOH M (1); YAJIMA K (1); OKUYAMA H (1); **SUZUKI T** (1); URUGA K (1)
(1) Fujikura Ltd., Tokyo, JPN
Proc 5th Int Microelectron Conf 1988, 1988, PAGE.27-32, FIG.8, TBL.2, REF.4
JOURNAL NUMBER: K19900585F
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

45/3,AB/4 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01091599 JICST ACCESSION NUMBER: 90A0596769 FILE SEGMENT: JICST-E
High-temperature, high-sensitivity pressure sensor using multi-layer SOI structures.
CHUNG G-S (1); KAWAHITO S (1); ISHIDA M (1); **NAKAMURA T** (1)
(1) Toyohashi Univ. Technology, Toyohashi, JPN
Tech Dig Sens Symp, 1990, VOL.9th, PAGE.39-42, FIG.7, REF.10
JOURNAL NUMBER: X0768ABH
UNIVERSAL DECIMAL CLASSIFICATION: 621.382:537.226.86 531.78
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

45/3,AB/5 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00082163 JICST ACCESSION NUMBER: 85A0248682 FILE SEGMENT: JICST-E
A GaAs FET low-noise amp module for DBS receivers.
MORI TETSURO (1); SAKAMOTO SUSUMU (1); FUJIOKA KOJI (1); IKEDA YASUKAZU (1); **SUZUKI TAKESHI** (1)
(1) Mitsubishi Electric Corp., Kitaitami Machinery Works
Mitsubishi Denki Giho, 1985, VOL.59,NO.3, PAGE.231-233, FIG.8, TBL.1, REF.4
JOURNAL NUMBER: F0198AAP ISSN NO: 0369-2302 CODEN: MTDNA
UNIVERSAL DECIMAL CLASSIFICATION: 621.375 621.397+654.197
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

45/3,AB/6 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

09576985 PASCAL No.: 91-0367426
Novel pressure sensors wtith multilayer soi structures
CHUNG G S; KAWAHITO S; ISHIDA M; **NAKAMURA T**
Toyohashi univ. technology, dep. electrical electronic eng., Tempaku-Cho, Toyohashi 441, Japan
Journal: Electronics letters, 1990, 26 (12) 775-777
Language: English

45/3,AB/7 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

08484032 PASCAL No.: 89-0032822
Low dielectric constant multilayer glass-ceramic substrate with Ag-Pd wiring for VLSI package
SHIMADA Y; **YAMASHITA Y**; TAKAMIZAWA H
Materials development cent., NEC Prefecture 213, Japan
Journal: IEEE transactions on components, hybrids, and manufacturing technololgy, 1988, 11 (1) 163-170
Language: English
De nouveaux composites verre-ceramique a faible constante dielectrique pouvant etre frittes vers 900 C dans l'air sont obtenus. On peut obtenir une resistivite electrique tres faible des conducteurs en controlant la forme des particules d'argent et de palladium. La construction electrique doit etre consideree pour ce qui est du substrat. Les proprietes de transmission de l'impulsion sont fortement influencees par la nature des plans de mise a la terre et des plans d'interconnexion. On mesure donc les proprietes fondamentales de transmission des impulsions, retard de propagation, impedance caracteristique, bruit de couplage par diaphonie, dans diverses structures a couches multiples. De nouvelles technologies de controle des proprietes de substrats sont etablies. On resume les caracteristiques du nouveau substrat en couches multiples de verre et ceramique. Le retard de propagation est petit grace a la faible constante dielectrique (epsilon =3,9); la resistivite electrique est faible et le cout peu eleve pour un systeme conducteur argent-palladium (<4 mu OMEGA cm); on utilise une construction electrique perfectionnee pour le controle d'impedance et de diaphonie; la methode de fabrication est tres precise

45/3,AB/8 (Item 3 from file: 144)
DIALOG(R)File 144:Pascal

03820042 PASCAL No.: 82-0342075
ADVANTAGES OF THERMAL NITRIDE AND NITROXIDE GATE FILMS IN VLSI PROCESS
ITO T; **NAKAMURA T**; ISHIKAWA H
FUJITSU LABORATORIES LTD./KAWASAKI 211,JAPAN
Journal: IEEE J. SOLID-STATE CIRCUITS, 1982, 17 (2) 128-132
Language: ENGLISH
DISCUSSION DES PROBLEMES INHERENTS A LA PRODUCTION D'ISOLANTS MINCES FIABLES (MOINS DE 200 A D'EPAISSEUR) CONVENANT POUR DES COUCHES MINCES DE GRILLE POUR L'INTEGRATION A TRES GRANDE ECHELLE. AVANTAGES DE COUCHES MINCES DE NITRURE DE SILICIUM GROSSIES THERMIQUEMENT ET D'OXYDE NITRURE THERMIQUEMENT ("NITROXYDE") PAR RAPPORT AUX COUCHES MINCES DE SIO SUB 2

01/31/2003

THERMIQUES

45/3,AB/9 (Item 4 from file: 144)
DIALOG(R)File 144:Pascal

03744735 PASCAL No.: 82-0264364
PHOSPHORUS-DOPED MOLYBDENUM SILICIDE FILMS FOR LSI APPLICATIONS
INOUE S; TOYOKURA N; **NAKAMURA T**; ISHIKAWA H
FUJITSU LABORATORIES LTD./KAWASAKI,JAPAN
Journal: J. ELECTROCHEM. SOC., 1981, 128 (11) 2402-2410
Language: ENGLISH
DISCUSSION SUR LES PROPRIETES DES COUCHES DEPOSEES PAR COPULVERISATION, LA COMPOSITION DES COUCHES, LE COMPORTEMENT DU PHOSPHORE, LES PROPRIETES ELECTRIQUES DU CONTACT ENTRE SILICIUM ET LE SUPPORT SI ET LES CARACTERISTIQUES DU DISPOSITIF MOS